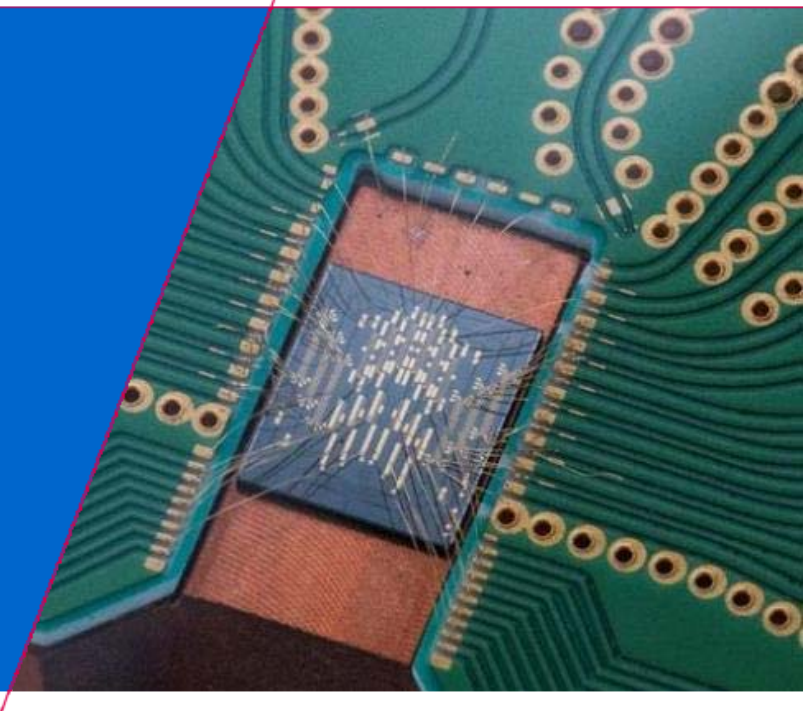
OpenPICs WP3
5th December 2016



JePPIX

TU/e Technische Universiteit Eindhoven University of Technology

Where innovation starts

Agenda Part I

WP 3.1 BB Design

WP 3.3 BB Characterization

WP 3.5 Demonstrator

WP 3.2 PDK Content

WP 3.1 BB Design

- **[Action] Technobis: Tunable laser specifications**
- **[Action] TU/e: Circulation of documents for BBs, project documents, list of deliverables/milestones, planning**

https://phi.ele.tue.nl/OPZuid/Documents/
login: opzuid
pw: atDuegsyu

OPZuid documents - partner area

Filename	Type	Size	Date Modified
MeetingNotes	<Directory>	<Directory>	Dec 1 2016 7:07 PM
Milestones	<Directory>	<Directory>	Dec 1 2016 6:55 PM
Reports	<Directory>	<Directory>	Nov 25 2016 3:37 PM
WP3_plan.xlsx	Spreadsheet	40.4 KB	Dec 1 2016 6:53 PM
WP4_plan.xlsx	Spreadsheet	22.5 KB	Dec 1 2016 6:53 PM

WP 3.1 BB Design

- [Action] Bright: Circulation of documents for BBs
- [Action] Bright: Include low range tunable laser into planning
- Structures for SP 19 from Bright
- Role of Lionix in WP3

WP 3.1 BB Design

MPW run	SP18		SP19			SP20			SP21			SP22			SP23		
MPW																	
	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb
	2016Q4			2017Q1			2017Q2			2017Q3			2017Q4			2017Q1	

MZM v1

SSC

Tunable laser?

DUV for filter?

RF lines?

WP 3.3 BB Characterization

- **[Action] Smart: Provide most up-to-date data on existing FoM measurements.**

1. **List of Building Blocks to be tested**
   a. **SOA**
   b. **EOPM**
   c. **Shallow/Deep WG + tapered versions**
   d. **AWG**
   e. **Photodetector**
   f. **MIRs**
   g. **MMIs**
   h. **Saturable Absorber**
   i. **Current injection tuning**
   j. **Electrical Isolation**
   k. **RF metal**

Generic test structures in openPICs

- **Different Test Structures**

Process Control (PCM)

- CD SEM
  - Etch depth
  - WG width
  - (WG gap)
- Layer stack definition
- PL intensity
- Wafer strain
- Sidewall roughness+angle

During process
On wafer

Wafer Verfication

- IV and LI curve
  - Cleaved FP laser bar
  - (FP laser with MIR)
- WG loss

Bar level
+optical alignment

- PCM and wafer verification to be tracked per run
- Gain statistical data

Generic test structures in openPICs

Different Test Structures

Building Blocks

- a. SOA
- b. EOPM
- c. Shallow/Deep WG loss

+ tapered versions

- d. AWG
- e. Photodetector
- f. MIRs
- g. MMIs
- h. Saturable Absorber
- i. Current injection tuning
- j. Electrical Isolation
- k. RF metal

- Most after cleaving in bar form + optical alignment
- Basic BBs can be organized with standardized pad placement for automated bar tester
- Targeted introduction of new BB test cell SP 20, march 2017
- Reuse for each MPW after that

- Several iterations of composite BB testing before release as IP block

WP 3.3 BB Characterization

- **[Action] TU/e + Smart: Structures for SP19**

1. Metal plating testing
   - DC conductivity
   - P-metal and n-metal connectivity
   - Slope reliability
   - Minimum width test
   - Minimum gap test
   - Differences in p-metal, n-metal, passivation etch metal reliability
2. Parameter Extraction
   - Sheet resistance p-InGaAs
   - Sheet resistance p-InP
   - Sheet resistance n-InP
   - PN junction IV curve
   - P-metal contact resistance
   - N-metal contact resistance

1. Modulator MQW stack testing
   - Butt-joint reflection test structure
   - Phase-shifter efficiency x L
2. Etch Process tests
   - Deep etch slope test
   - Shallow etch slope test
   - Passivation flatness over deep trench

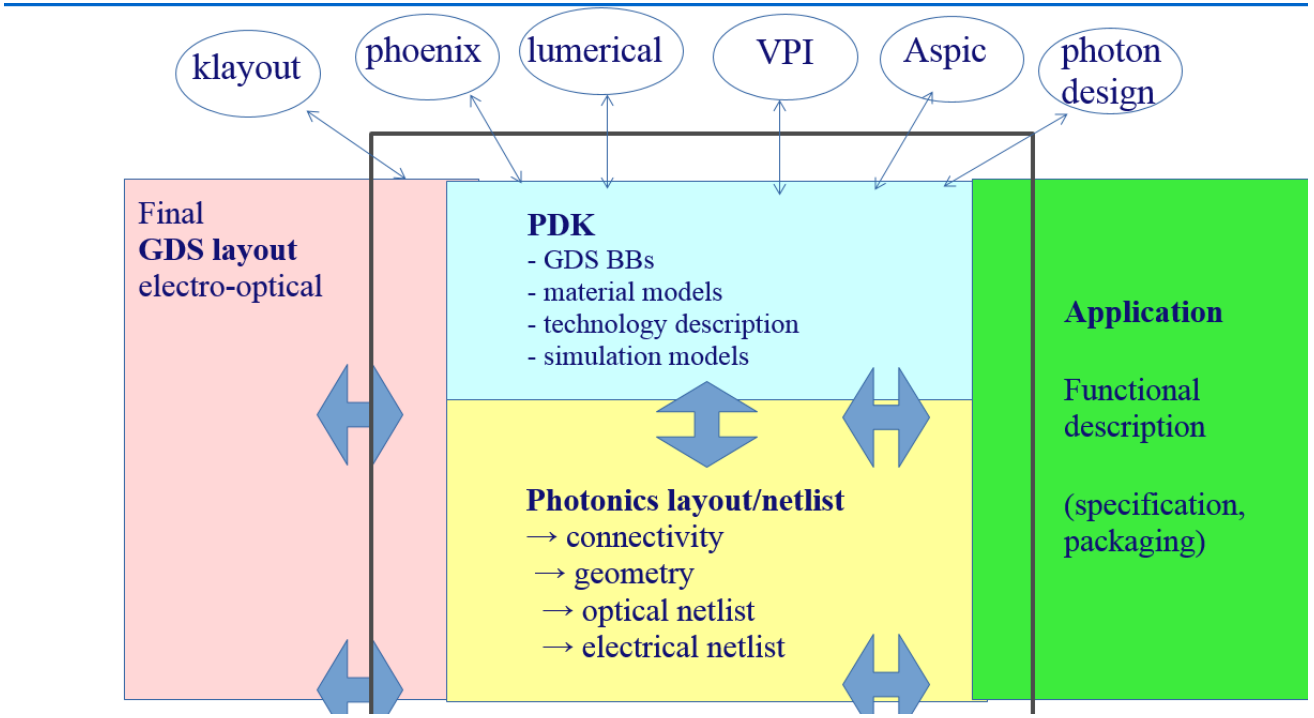
WP 3.5 Demonstrator – tunable laser

For SENSING APPLICATION 1 (LDG // PLG)					
Specification	Priority	Requirement			unit
		Min.	nominal	max	
Central wavelength (default)	Must	1535	1550	1565	nm
Modulation range (peak peak)	Must	1	10		pm
	Should		1500		pm
	Could		10	50	nm
Modulation frequency (with nominal peak peak)	Must	10	100		Hz
	Should	1.000	10.000		Hz
	Could		1		MHz
Tuning range	Must	1	2		nm
	Should	5	10		nm
	Could		50	100	nm
Tuning speed	Must	10			pm/sec
	Should		1		nm/sec
	Could		10		nm/sec
Linewidth	Must		100	900	kHz
	Should		40		kHz
	Could		1		kHz
Output power	Must	1			mW
	Should		10		mW
	Could		50		mW

For SENSING APPLICATION 2 (CRT // PLG)					
Specification	Priority	Requirement			unit
		Min.	nominal	max	
Central wavelength (default)	Must	1535	1550	1565	nm
Modulation range (peak peak)	Must	0	1		pm
	Should		100		pm
	Could		1.5	50	nm
Modulation frequency (with nominal peak peak)	Must	1	100		Hz
	Should	1.000	10.000		Hz
	Could		1		MHz
Tuning range	Must	1	2		nm
	Should	5	10		nm
	Could		50	100	nm
Tuning speed	Must	10			pm/sec
	Should		1		nm/sec
	Could		10		nm/sec
Linewidth	Must		10	40	kHz
	Should		1	20	kHz
	Could		1		kHz
Output power	Must	1			mW
	Should		10		mW
	Could		50		mW

WP 3.2 PDK Content

- **[Action] Bright and Phoenix: Circulate “what belongs to PDK”.**



Agenda Part II

- **WP 3.4 Design Environment**

WP 3.4 Design Environment

- **[Action] Bright and Phoenix: Circulate design flow model**
- **[Action] TU/e: Revised WP 3.4 Plan + Milestones/Deliverables**

WP 3.4 number	Design Enviroment M or R title	Description	items	Responsible		
M0	Status of design flow	Outline presenting design workflow and procedures, identifying points of improvement	1x	Phoenix	Marcel	Phoenix, Smart, TU/e
M1	Design flow improvement concept	present the concept of the improvements to be worked on	1x	Phoenix	Marcel	Phoenix, Smart, TU/e
R0	Standardized templates for establishing compact models	Detail the concept and requirements for compact models for BBs	1x	Phoenix	Marcel	Phoenix, Smart, Bright
R1	Advancement of DRC functionality	improving on present DRC capabilities in design flow cycle	1x	Bright	Ronald	Phoenix, Smart, TU/e
R2	Improvement of mask level software capability	Improving tools that work on mask and layout level to facilitate design procedure	1x	Bright	Ronald	Phoenix, Smart, TU/e
M2	Convergence of design enviroment	Achieving closer interplay between design tools and enviroments	1x	Phoenix	Marcel	TU/e, Smart, Bright