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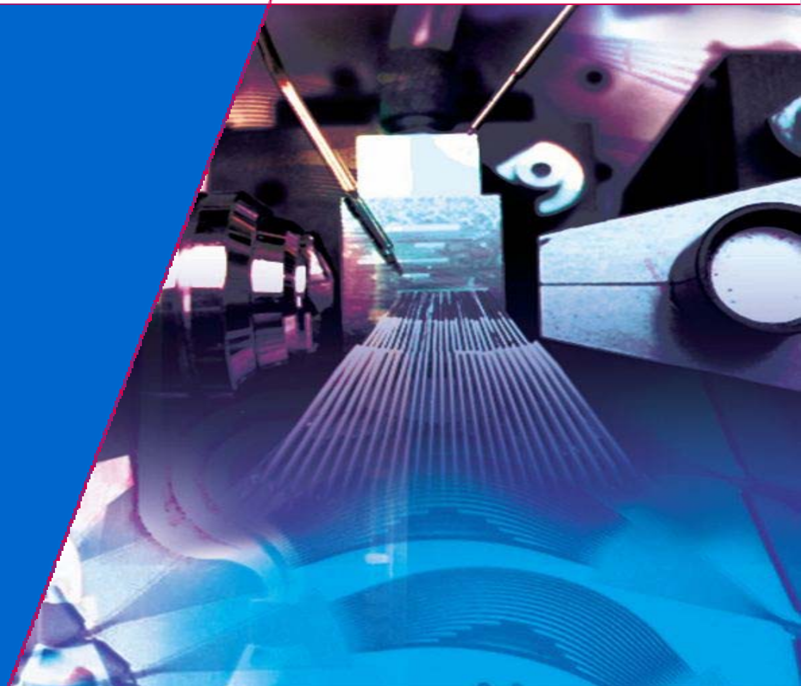
OpenPICs WP 4

Planning and targets



Institute for Photonic Integration
Materials · Devices · Systems

TU/e Technische Universiteit Eindhoven University of Technology

Where innovation starts

Technology to-do list

Development

Technologies to be developed	Initial test	JTC run validation	Smart MPW validation	Smart MPW commercial
SI-substrate process				
Metal plating				
Modulator MQW epi				
SSC stack and process				
DBR process				
DUV scanner process				
Zn in-diffusion epi				
Al-MQW epi				
Thick insulation & opening				
Stepper process				
CMP process				

Work plan overview

Technologies	Schedule of introduction											
	2016	2017				2018				2019		
	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
SI-substrate process												
Metal plating		?										
Modulator MQW epi				Pending								
SSC stack and process				Pendi ng								
DBR process		EBL	DUV									
DUV for WG definition	Plan											
Zn in-diffusion epi												
Thick insulation & opening												
Al-MQW epi												
Stepper process												
CMP process												

Initial test | JTC run validation | Smart MPW validation | Smart MPW commercial

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Effort resources

Technical tasks	FTE allocation							Resources	
	Longfei	Tjibbe	Robert	Rene	Smart	Lionix	Total fte	OpenPICs	Other projects
MQW epi and process (P- and Al- based)	0.6		0.1		0.2		**0.9**	WP 4.1	Florian (GeTPICs) Jorn (Gravitation)
Thick insulation and contact opening	0.2	0.2	0.1				**0.5**	WP 4.3	Arezou (Photronics) Robert (NextGen)
Zn in-diffusion A/P integration		0.2		0.2			**0.4**	WP 4.1	Jon, Simone (ECO group)
Stepper process			0.2				**0.2**	WP 4.3	Equipment technician (Nanolab)
DUV process					0.7	0.3	1	WP 4.2	Jereon (new STW project)
Total fte	**0.8**	**0.4**	**0.4**	**0.2**	**0.9**	**0.3**	**3**		

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MQW epi and process (1)

- P-QWs epi and process
  - **Motivation:** for modulators >20 GHz
  - **Plan**: Effect epi → Smart MPW 2017 Q1
  - **Challenges**: IP issue

- Al-QWs epi and process
  - **Motivation:** for modulators >40 GHz
  - **Plan**: QWs design (WP3) → growth (Smart) → process for regrowth (Longfei) → JTC run with shallow-etch modulator design (2018 Q1, Tjibbe)
  - **Challenges**: Al-QWs (wet) etching, butt-joint quality, Al oxidation
  - **Schedule**: 2017 Q1 – 2018 Q1
  - **Other resources**: Al-based PIC fabrication (Florian)

MQW epi and process (2)

- Regrowth rabbit-ear optimization *(depends on NextGen results)*
  - **Motivation:** for DUV litho optimization
  - **Plan**: Wafer with full epi (Smart) → CMP (Robert) → JTC run with DUV WGs (2018 Q3, Tjibbe)
  - **Challenges**: CMP process for InP
  - **Schedule**: 2018 Q1-Q3
  - **Other resources**: NextGen project using CMP for DUV optimization (Robert)

- Al-etch and passivation
  - **Motivation:** for deep-etch only process, low RF loss in modulators, insights for full Al-platform.
  - **Plan**: Wafer with full epi (Smart) → deep etch and sulfide passivation (Longfei) → JTC run with deep-etched BBs (P- or Al- based) (2019 Q1, Tjibbe)
  - **Challenges**: Al-QWs (dry) etching, passivation
  - **Schedule**: 2018 Q1 – 2019 Q1
  - **Other resources**: Al-QWs deep-etch and passivation (Yuqing, Jorn)

Thicker insulation and contact open

- Polymer insulation and open
  - **Motivation:** for high-speed RF lines
  - **Plan**: 5 µm BCB or Polyimide spin (Tjibbe) → CMP (*optional,* Robert) → Etching slopes/vias (Tjibbe) → metal plating (Tjibbe) → JTC run (2017 Q3, Tjibbe)
  - **Challenges**: deep etch, polymer uniformity/CMP process, polymer reliability
  - **Schedule**: 2017 Q1-Q3
  - **Other resources**: Photronics project: thick BCB process (Tjibbe, Arezou)

- Oxide insulation and open *(under discussion)*
  - **Motivation:** for reliable insulation (CMOS standard process).
  - **Plan**: SiO2 deposition (PECVD/HDP) → CMP (Robert)
  - **Challenges**: Stress in SiO2 deposition, CMP process
  - **Schedule**: 2018 Q1 – 2019 Q1

Zn in-diffusion and JTC validation runs

- Zn in-diffusion A/P integration
  - **Motivation:** for low loss WGs and RF lines
  - **Plan**: diffusion tests and measurements (Rene) → JTC run (2017 Q3, Tjibbe)
  - **Challenges**: impact on active devices
  - **Schedule**: 2017 Q1-Q3
  - **Other resources**: Fabrication runs in ECO (Jon, Simone)

- JTC validation runs
  - **Motivation:** for validating the process developed in JTC
  - **Responsible**: Rene (epi), Tjibbe (process), and design teams
  - **Plan**: 2017 Q3 (Zn diffusion, planarization) → 2018 Q1 (Al MQW, stepper) → Q3 (CMP) → 2019 (deep-etched BBs, Al platform) …

Stepper and CMP process

- Stepper process
  - **Motivation:** for high-yield industry-standard lithography
  - **Plan**: photoresist tests (Robert) → process tests (Robert) → JTC run (2018 Q1, Tjibbe)
  - **Challenges**: equipment out of service
  - **Schedule**: 2017 Q1-Q4
  - **Other resources**: new stepper in Smart, new equipment technician support

- CMP process
  - **Motivation:** for rabbit-ear removal, uniform insulation layer
  - **Responsible**: Robert
  - **Plan**: tests for InP and BCB (2017), tests for SiO2 (2018)
  - **Other resources**: NextGen project using CMP for DUV optimization (Robert)

Parameter matrix: Epitaxy related (4.1)

Design parameters			Process parameters (required)					
Building blocks	Figures of merit	Target values	Epi. thickness variation	Epi. index variation	QW E-O coefficient	Butt-joint reflection (dB)	P-cladding doping (cm^{-3})	Contact resistance (Ω cm^2)
High-speed modulator	EO bandwidth	20, 40, 80 GHz			x			~1E-6
	Vπ value	~2 V	x		x			
	Insertion Loss	< 6 dB				x		
High-speed RF-line	Bandwidth (3 dB)	> 40 GHz					x	
	Impedance	50 Ω						
Spot-size converter	Coupling loss	< 1 dB	x	x				
	Spot size	4x4 or 10x10 um^2						
High-precision filter	Wavel. accuracy	< 1 pm	x					
	Insertion loss	< 1 dB						
	Cross-talk	< -40 dB						
Low-linewidth tunable laser	Linewidth	~100, 10, 1 kHz				< -50	x	
	Tunable range	> 30 nm						
	Output power	> 10 dBm		x				x
Low-loss WGs	Propagation loss	< 1 dB/cm	x	x			x	
Current process capabilities			Core: 500 nm ±10%	PL: 1550±15nm 1250±40nm	phosphide -MQW	-40 (straight) -50 (angled)	1E+18	N: <1e-6 P: 2~3E-6
Potential process solutions					Al-MQW		Selective Zn diffusion	

Parameter matrix: RF lines related (4.3)

Design parameters			Process parameters (required)					
Building blocks	Figures of merit	Target values	Polymer thickness (µm)	Polymer thickness variation	Metal thickness (µm)	Contact alignment accuracy (µm)	Metal separation min. (µm)	Metal width min. (µm)
High-speed modulator	EO bandwidth	20, 40, 80 GHz	> 5 µm		> 1	<1	3	
	Vπ value	~2 V						
	Insertion Loss	< 6 dB						
High-speed RF-line	Bandwidth (3 dB)	> 40 GHz	> 5 µm	x	> 1			3
	Impedance	50 Ω	x	x	x			
Spot-size converter	Coupling loss	< 1 dB						
	Spot size	4x4 or 10x10 um^2						
High-precision filter	Wavel. accuracy	< 1 pm						
	Insertion loss	< 1 dB						
	Cross-talk	< -40 dB						
Low-linewidth tunable laser	Linewidth	~100, 10, 1 kHz						
	Tunable range	> 30 nm						
	Output power	> 10 dBm						
Low-loss WGs	Propagation loss	< 1 dB/cm						
Current process capabilities			0.4	±3%	0.4	1	5 (TBD)	5 (TBD)
Potential process solutions			Extra layer thickening	CMP ?	Plating (>2)	Stepper (<0.5)	Lift-off optimization	

Parameter matrix: DUV related (4.2)

Design parameters			Process parameters (required)			
Building blocks	Figures of merit	Target values	WG width min. CD (μm)	WG width CD variation	Side-wall roughness (nm)	Etch depth variation
High-speed modulator	EO bandwidth	20, 40, 80 GHz	1	x		
	Vπ value	~2 V				
	Insertion Loss	< 6 dB			x	x
High-speed RF-line	Bandwidth (3 dB)	> 40 GHz				
	Impedance	50 Ω				
Spot-size converter	Coupling loss	< 1 dB	0.4	<<0.05 μm	x	
	Spot size	4x4 or 10x10 um^2				
High-precision filter	Wavel. accuracy	< 1 pm	0.2	x		
	Insertion loss	< 1 dB			x	
	Cross-talk	< -40 dB				x
Low-linewidth tunable laser	Linewidth	~100, 10, 1 kHz		x	x	
	Tunable range	> 30 nm				
	Output power	> 10 dBm			x	
Low-loss WGs	Propagation loss	< 1 dB/cm	x	x	x	x
Current process capabilities			1.5 μm	±10%	TBD	±30 nm
Potential process solutions						