**Minutes from OpenPICs Review Meeting 09/10/2018**

Present: Weiming Yao, Kevin Williams, Victor Calzadilla, Aura Higuera, Rob Geertman, Vincent Docter, Saeed Tahvili, Ronald Broeke, Marcel van Vliet, Joost van Kerkhof (call)

Time: 13:00-17:00

**State of the Project**

- Internal meeting: review progress and agree on how to organize the rest of the project
- Since start, administrative and technical report submitted every half year
- Stimulus clarified that the project finishes Dec 2019
- Final report December 2019, Weiming suggest to keep original planning and get it done in Aug 2019

**WP1**

- Participation in events and promotional activities outlined
- Advertisement of JePPIX Trainings
- Roadmap and survey results mentioned
- MPW server will be extended

**WP2**

- Database created for instances: breakage, contamination, reduced performance, in order to better track quality of wafer runs. Every product is traced now.
- Project light year ongoing: goal is stabilized process with high reliability
  - Plan of 40 wafers with no influences, changes, exactly the same → reproducibility.
- SP22-A-03 3rd time wafer run
- SP23-A-03 2nd time wafer run
- SP25-B and SP26-B cancelled. Next B run is SP27-B
- R&D working in: new way to generate WGs and contact opening and removal with less steps more reliable, independent layers
- The whole cycle should be optimized with decoupled process steps. Different depths in etching are separated, not connected to each other.
- SP24-B delivery end of 2018
- DBR laser available
- All MPW B runs don't affect platform behaviour. Report on SI-substrate influence by the end of this year.
- SSC development more difficult than expected, 1st in SP22 not good enough. Rerun in SP23B.
- SSC characterization results not extensively characterized and under performance.
- SP21,22,23 Threshold current 20-25 mA, Optical power 75 mW

**WP3**

- For SSC BB, design from other project is used. Might reconsider spending effort on design in OpenPICs
- PDK content: figure of merits defined, compact model report to follow (Rui, addition after talks with Smart)
- BB test cell results presented

- Execution flow: included at the start of the planning, handle data gathered in measurement labs and connect to chip and wafers
    - TU/e develops a framework for execution flow
- Modulator: 20, 40, 80 GHZ EO bandwidth targeted at start of project, 30 GHz achieved so far
    - For SP24: test structures to explore capacitive loading concepts have been implemented
- RF Lines
    - No BB yet on SI-InP runs. Developed an N-InP RF block, loss limited by substrate.
    - BCB RF Lines show reduced loss by using thick insulating material on top. Dielectric 7 µm thick
    - Decouple electrical routing and optical routing
- BB Characterization
    - Creating infrastructure for automated setup, multi contact probe card, image recognition. Standardize electrical interface on the chips
    - Status: almost demonstrating calibration step and automatic alignment.
    - Electrical WG loss measurement with DBR laser and ring resonator
- Execution flow
    - Data write module with meta data in YAML format
    - Data tagging by Bright photonics
- Phoenix
    - Focusing in design flow improvements.
    - Black box replacement and auto routing. Complex designs go well.
    - SMART PDK release with compact models
    - PDA flow status not fixed after the synopsys acquisition. Future to the PDA flow foundation not decided
    - Marcel is interested in JSON format of building blocks from Ronald
    - Problem with ADS implementation. Compiling versions not neat. Info of PDK should be in independent way, operating system.
    - DRC improvements: feedback form costumers and implemented DRC grouping.
    - DRC can take up to days, work to speed it up.
    - Optodesigner can export in GDS with additional information to the net list.
    - Scalability of DRC, making DRC parallel, what can be done at the same time at diff cores of the computer.
- Bright Photonics:
    - Developing PIC design flow with Nazca, stabilized flow now
    - High quality, closed-end user loop mask assembly and DRC
    - BB block development prototypes
    - BB design:
    - High precision filter, low linewidth tunable laser, low loss passive waveguides offset/ bends
    - Tool independent foundry definitions
    - Nazca integrating with VPI.

**WP4**

- AL-MQWs grown no much difference form expected values of wavelength

    - Wafers grown were with no strain and with strain
    - AP integration check looks ok, plan for full modulators
    - Oxidation at active interface, maybe TEM to check? Samples need to be prepared.
    - Cleaving already oxidizes, maybe cleave with FIB.
    - Temperature cycling, chicken test with passivation test samples did at EFFECT photonics.
    - SiOx used because SiN showed to be craking in the past
- Zinc diffusion:
    - Zinc diffusion is a no go after reviewing results.
    - Diffusion obtained in InP and InGaAs but not enough control
    - Negligible interstitials
- RF lines on top of 7 µm thick insulation. Fabrication of front runner.
    - 1st idea remove BCB where not needed. Problems because of non-uniformity and topology.
    - Remove the BCB only when needed removed (cleaving lines, metallization)
- Stepper processes
    - MAN resist available in stepper
    - Positive resist AZ to cover most of wafer while dry etching some areas
    - MIR701 tested to etch WGs with the scanner
- **Lionix**
    - Orthogonal activities to the project.
    - Run in openpics project to test BBB determine DUV litho proves to improve performance of small features components
    - Operational issues to get access to CR in Eindhoven.
    - Scanner run is planned. Equipment was not compatible because dedicated reticle was needed. Reticle will be ordered next week.
    - BBs already existing with performance data of contact lithography and stepper litho. AWGs, splitter functions.

**Demonstrators**

- Technobis
    - Scanner stepper and SSC most important
    - Based on an existing product but higher resolution WGs, initial target SP26B shifted to SP28B now.
    - Await results of SP23B SSC with diluted waveguides
- Effect Photonics
    - 8X50 Gbps or 4x100 Gbps PAM 4
    - 8x50 level of integration is high
    - Wavelength multiplexer AWG trouble with higher integration, not nice tunable laser, you need a way to multiplex the 8 channels together. Is tricky with the AWG.
    - 4x100 Gbps PAM 4 less components, favorable for package size and power consumption. Linewidths are higher. It's becoming the industry standard. You occupy more spectral space.
    - The vendor of drivers are doing this schematic. 4 lasers combining them could be easier. Wavelength independent power combiner like MMI splitter. Specs wise 4x10 is in scope.

- RIN of the laser, junction's reflections, modulator Vpi is the same for both designs.
- PAM4 still dependent of the Si chip (driver), energy of the module. Dispersion penalty is considered.
- DBR I nm tuning range is difficult to hit the channels so difficult for the 4 channel solution.
- CPW modulators, BB available. Reflection S11 is a huge mismatch and won't give the performance for high baudrate. The BB is good for single channel but for multichannel is not good enough.
- **Approach by Effect:**
- Optical subassembly module, power goes to cooling and DSP, rest PIC TX.
- Reasonable to use big pads double wire bonds.
- Main decision on design is about minimum mechanical routing tolerances while keeping RF performance
- Photonic IC: 4 channels 4x6 mm, thermistor on PIC, -5dBm output power expected
- RIN <140 dB/Hz
- MZM BW >35 GHz
- Focus on SP27B (15 feb 2019 tape-out, delivery June 2019), diff design on lasers and modulator with and without RF lines.