Open Innovation Photonic ICs

OpenPICs

Technical Summary Report

(09/2016 – 06/2017)

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Introduction

Photonic Integrated Circuits (PICs) are key enablers for data transmission and sensing in the More than Moore paradigm. These integrated circuits process light to exploit the massive bandwidth, energy efficiency as well as phase and polarization properties of light for more precise measurements. Historically, PICs have been first applied in the telecom area as the transmitter and receiver devices that send information through optical fibre. In recent years, with the explosive growth of internet services, photonic circuits are extensively used there for information transfer and processing, enabling a reduction in power consumption and an increase in efficiency and performance. In addition, PICs are opening up new possibilities, in fields such as health care, biological imaging and the monitoring of mechanical structures. The North Brabant region is a leader in the field of photonics and is home to leading research facilities and an innovative photonics industry. With the Open Innovation Photonic IC (OpenPICs) project, participating partners strengthen this position by providing a strong industrial platform for PIC production for a new wave of PIC-enabled products.

The technology for the production of photonic circuits still needs to be optimized, both in terms of design as well as manufacturing processes. At present, several technological challenges need to be overcome to make this technology suitable for a wider uptake and to lay the foundation for capitalizing on the opportunities. The OpenPICs project addresses these issues and is organized around the following four work packages:

1) Market Demands

2) Process Characterisation

3) Building Block Improvement

4) Process Improvement

This technical report gives a summary of the major activities undertaken within the listed four work packages between September 2016 and June 2017.

Work Package 1 - Market Demands

Milestone Summary (WP1.M1): Linking Products to Building Blocks

Author: Weiming Yao

Goals

The generic integration platform for photonic integrated circuits provides mature building blocks that can be used to construct complete systems for product development. However, this technology push approach needs to be complemented by a market pull initiative, where products are identified that have significant market impact and their specifications are then mapped to building block requirements, giving focus to R&D efforts. The goal of this activity is to relate promising products to building block definitions and metrics.

Achievements

- Together with Technobis and Effect Photonics, we have identified two products as very promising with high impact market potential, namely the fiber sensor interrogator and the optical transmitter.
- We agreed on high-level specifications and system architectures of both applications so that the required subsystems in form of building blocks are defined.
- In case of the fiber sensor interrogator unit, a widely continuous tuneable laser with low linewidth is desired in combination with a high-precision filter. This requires improvement in the MZI, AWG and grating filter building blocks.
- In case of the optical transmitter, seamless integration of a tuneable laser and a high-speed modulator building block are desired. Both the laser and modulator performance need to be improved as well.
- More details are reported in the milestones WP3.5.R0 and WP3.5.R1

Milestone Summary (WP1.M2): Survey of requirements and building blocks

Author: Weiming Yao

Goals

The generic integration platform offers a wide range of basic and composite building blocks that need to undergo continued development towards higher performance and lower cost. In order to identify the most demanded building blocks and the amount of information the process design kit (PDK) should contain, we perform a technical survey with our expert partners.

Achievements

- We designed and created an extensive survey with the purpose to gather information on all available building blocks in the Smart Photonics generic platform.
- We received over 35 detailed responses from both academia and industry that give us insightful information.
- New technical insight was gained by analysing the preferred building blocks and their specifications.
- New business insight was gained through analysing the preferred cost per chip and cost for additional PDK information metrics.
- The survey acts as a valuable input for the platform roadmap in both the short and long term.

Figures

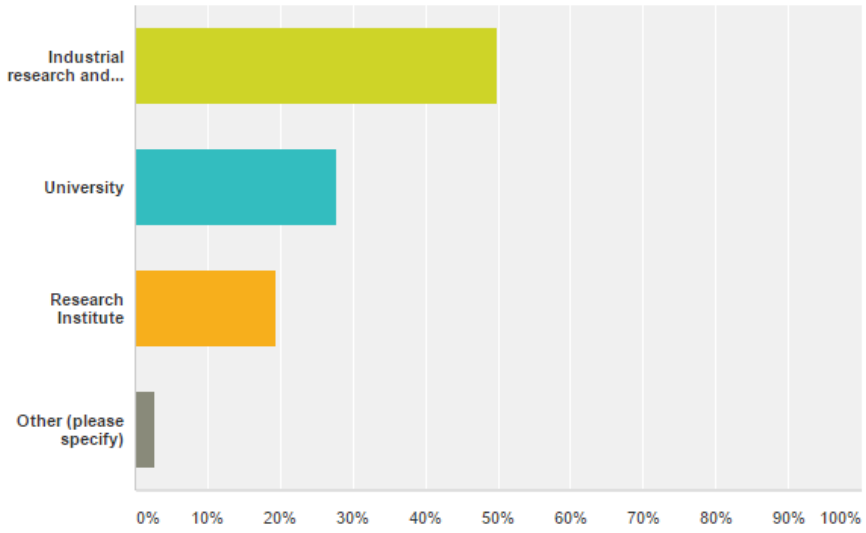


Figure 1: Distribution of surveyed parties. University and research institutions are equally involved as industrial research.

Milestone Summary (WP1.M5): Training and Outreach

Author: Aura Higuera Rodriguez

Goals

Reach out activities for PICs on open access InP platforms

Achievements

- More than 20 entities scouted:
  - SMEs
  - Universities
  - Mid-caps , corporates and multi-nationals
- Main topics:
  - Data-com (tuneable sources, C and L band operation in same chip)
  - Tele-com
  - Sensing (fiber sensing, gas sensing)
- Events participation and organization
  - PIC international 2017
  - OFC 2017 workshop and exhibition
  - World Technology Mapping Forum
  - ECOC 2017 workshop
- Trainings
  - JePPIX training in Beijing 2016
  - JePPIX training in Eindhoven 2016
  - Joint training with 7Pennings in LA 2017
  - JePPIX training 2017 Netherlands
  - JePPIX training China 2017 (work in progress)
- Outreach to users for feedback:
  - Well-developed generic platforms (more and more efficient BBB)
  - Reliability
  - Punctuality of MPW runs
  - Feasibility of PIC designs
  - Deep description of modules
    - Statistics of functioning
    - Modelling

Work Package 2 – Process Characterisation

Milestone Summary (WP2.M0.1): WP2 Project Charter

Author: Roel Daamen, Rob Geertman

General	
Project Name:	**WP2: Tracking and Process Improvement of Existing Building Blocks and Introduction of New Building blocks into the MPW**
Project Sponsor:	Stimulus OpenPICs
Project Manager:	Rob Geertman

Business Case Statement
[Why is the project being undertaken? What is the background of this project? What is the cost/benefit of the project?] **SMART:** **Process- and PDK-improvements of Generic Building Blocks and Extension of the library with new Building Blocks is essential for the success of SMART as a foundry.** **OpenPICs:** **The project promotes process development and ensures that a technological edge is maintained through innovative building blocks, processes and products for use by end users.** Cooperation with TU/e and other members of OpenPICs. Introduce and improve processes of Generic Building Blocks to a maturity level ready for PDK introduction.

Problem Statements
1. Functionality of Initial BB is proven, but stability over time is not yet proven
2. New BB introduced on existing MPW should not interfere with existing BB quality
3. Current maturity level of Process flow or existing BB's is not yet high enough

Goal Statement
1. Improve on the stability/variation on the current set of BB's (baseline)
2. Reach predefined quality level, specified for new BB's, without interfering current parameters
3. Incorporate new BB's into the standard MPW flow (baseline update)

Project Scope

Deliverables:

- Track BB parameters in available BB's (WP2.1)
- Improve quality and variation in available BB's (WP2.2)
- Introduce new BB's in the MPW (and PDK) with predefined quality (WP2.3)

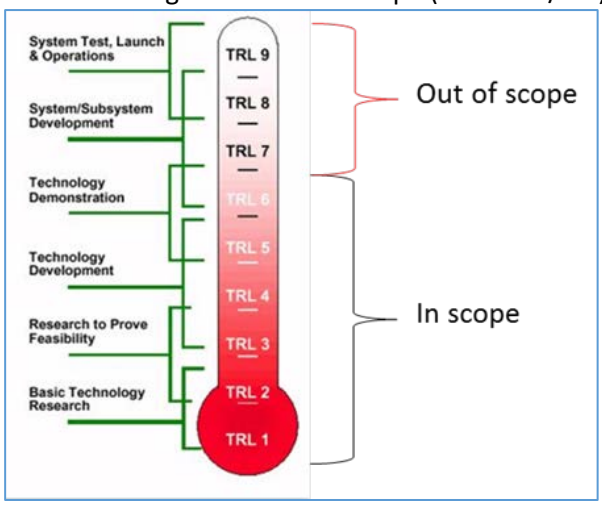
Assumptions: [What is the team assuming to be true?]

- Initial BB quality is within reach of SMART's capabilities (e.g. acceptable quality products with goo d uniformity) with current and/or to-be updated tool set

Constraints: [What are the limiting factors such as the budget or deadlines?]

- Limited set of information due to MPW-run approach
- Old equipment set not always ideally suited to get stable performance
- Smart' organization and man power is in the build-up phase

- **Out of Scope:** [What will be excluded from this project?]
- Manufacturing Yield is out of scope (i.e. TRL7t/m9)



- MPW process is still under improvement, this could interfere with the quality of BB's

High-Level Project Risks

- Complex processing and design interaction could lead to less-usable BB's or at an unacceptable low performance (potentially longer development time needed for decent performance)
- Internal communication with many partners, limited project management experience. Hence, timely delivery of new BB's is ambitious

Stakeholders & Affected Business Areas [Who will be impacted by this project?]

- SMART as a foundry, partners at OpenPICs

Core Team Members

- Roel Daamen (0.7), Rob Geertman (0.1), Erik den Haan (0.1), Kostas Voutyras(0.3) (all Smart Photonics)

Milestone Summary (WP2.1.M1.2): Generic MPW Planning & Update Q3'16 - Q2'17 Data

Author: Roel Daamen

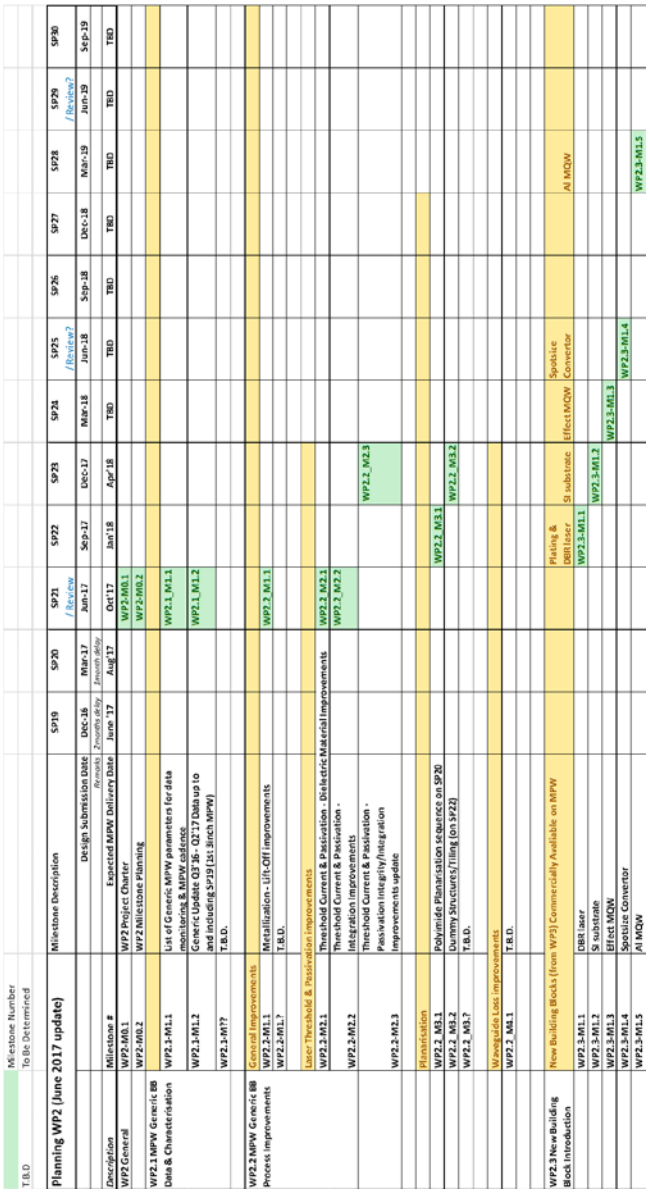
Goals

Show initial WP2 Milestone planning and related MPW cycle.

Achievements

- Initial WP2 Milestone Planning & MPW cycle available.

Figures



Milestone Summary (WP2.1.M1.1): List of Generic MPW parameters for data monitoring and improvement

Author: Roel Daamen

Goals

Define the initial list of Process/Performance Parameters that will be tracked to improve the MPW's as part of OpenPICS.
Schematically describe the approach to get to a better controlled MPW performance

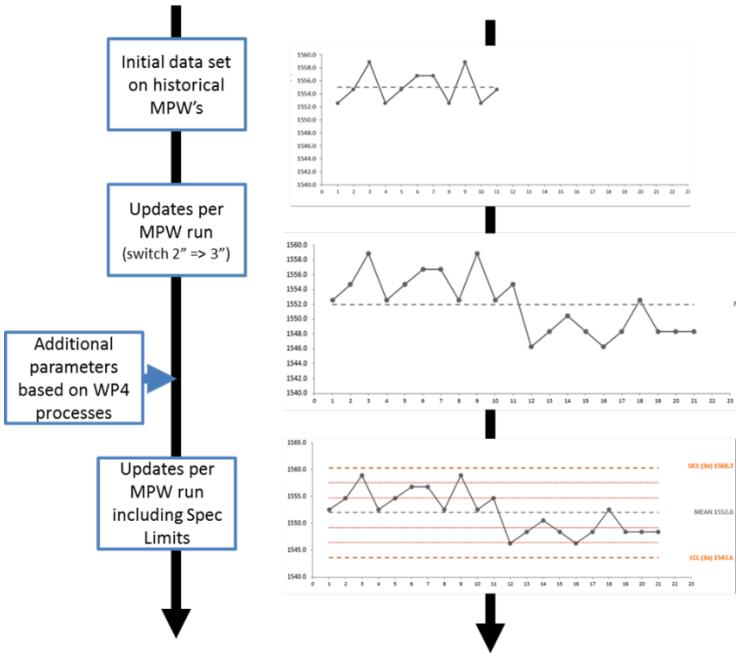
Achievements

- Initial list of Parameters has been selected
  - Will be populated with more items during the course of the project
- Schematic approach of New BB introduction

MPW & BB parameters

1) *Epitaxy*
2) *Waveguide Processing*
3) *Building Block Performance*
4) *Extend data set with New BB's (from WP3)*

Approach of new BB introduction & Approach for Spec Limits



Milestone Summary (WP2.1.M1.2): Generic MPW Parameters – Update Q2-2017

Author: Roel Daamen

Goals

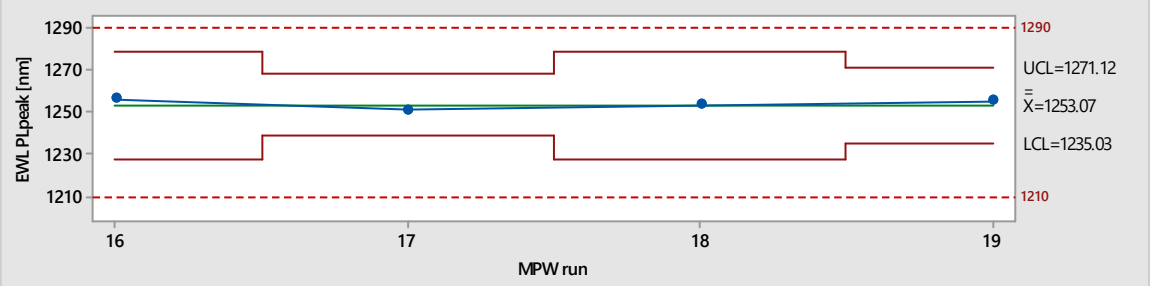
Track the MPW performance indicators over time to improve process stability

Achievements

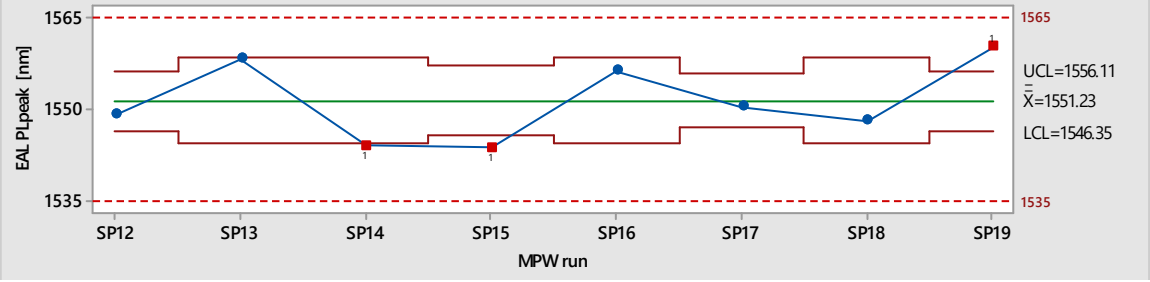
- Generated historical MPW data available for few selected items from Epitaxy (Active PLpeak, Passive PLpeak), Processing (Shallow Waveguide Width and BB performance (Waveguide Loss and Laser Threshold Current)
  - Will be populated with more items and limits during the course of the OPENPICS project

MPW & BB parameters per MPW run

- Epitaxy: Passive Layer PLpeak
  - Current Target 1250nm ±40nm
  - SP19 is 1st 3inch wafer MPW run using the L-reactor



- Epitaxy: Active Layer PLpeak
  - Current target 1550nm ±15nm
  - SP19 is 1st 3inch wafer MPW run using the L-reactor



Milestone Summary (WP2.1.M1.1): Generic BB Improvements – Metallization Lift-off

Author: Roel Daamen

Goals

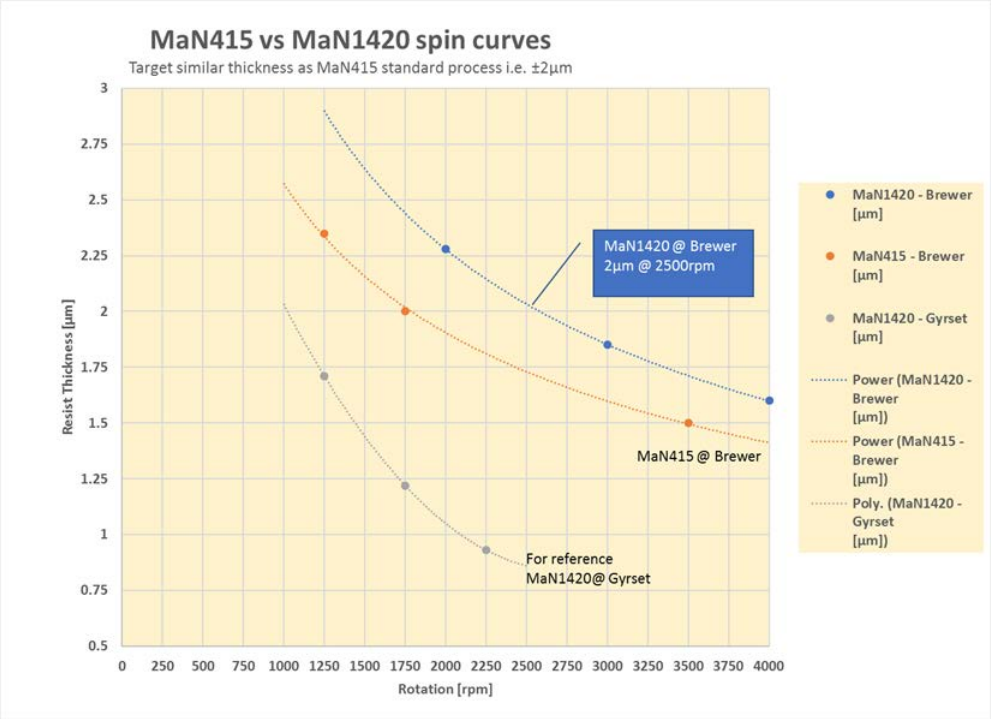
Reduce Metal Residues remaining after the Lift-Off process & Improve Narrow Line CD performance. Process should be applicable for Metals deposited by Evaporation & Sputter deposition

Achievements

- A process assessment was carried out on the existing Lift-Off Resist (LOR) process (i.e. MaN415)
- A new LOR with better Thermal Properties (higher Tg) was selected (MaN1420)
- The new LOR was successfully applied on InP wafers with Full Topography resulting in a new and improved Lift-Off process with reduced metal residues
- Critical Dimension (CD) performance of the MaN1420 at targeted line widths of 2.5 and 5µm has dramatically improved

Figures

- Spin curves of old MaN415 and new MaN1420 LOR



MaN1420 Process target @ 2500rpm to match Original MaN415 thickness

Milestone Summary (WP2.2.M2.1): Generic BB Improvements: Threshold Current & Passivation - Dielectric Material Quality

Author: Roel Daamen

Goals

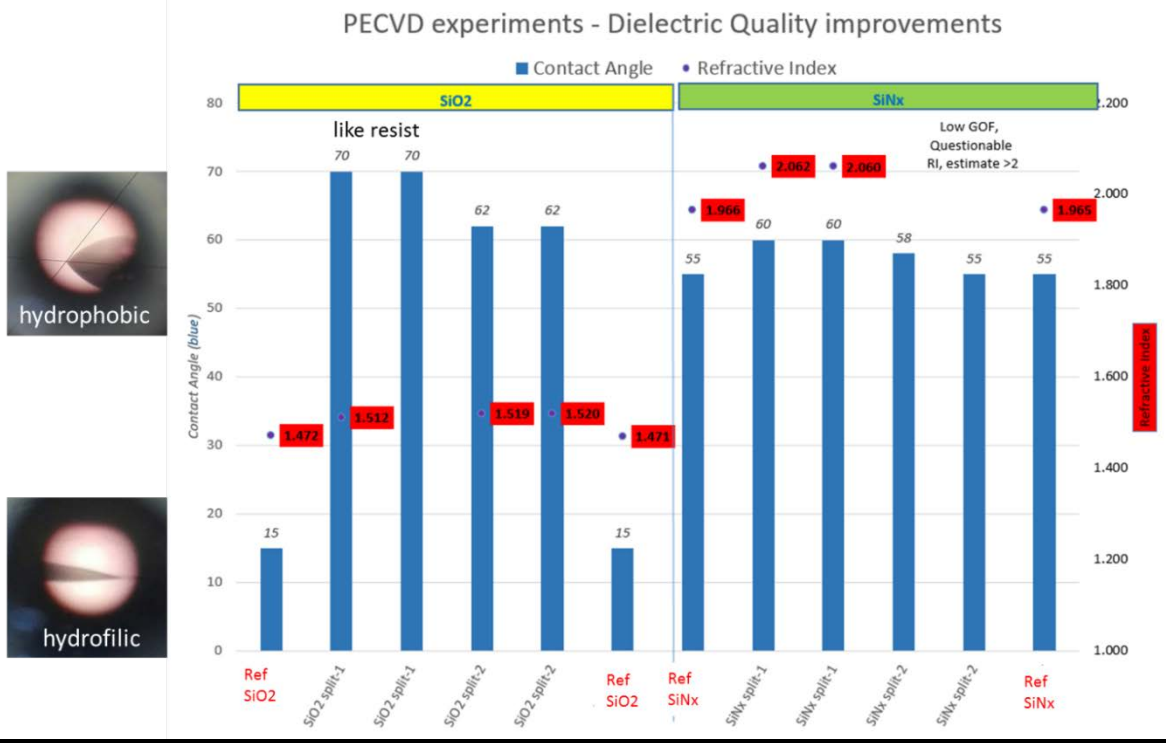
Current dielectric materials SiO2 and SiNX are of relatively poor quality, especially SiO2 has high leakage and is prone to absorb moisture.
Goal is to obtain higher Quality SiO2 (and SiNx) dielectric materials to be used for an Updated/Upgraded Passivation.

Achievements

- Contact Angle of SiO2 has been improved form a hydrophilic 15° to a hydrophobic contact angle >60°, small SiNx improvements. Contact angle stays stable over time
- Dielectric Breakdown improvements in SiO2 Split-1 removing all early fails around 85V with consistent breakdown occurring >160V
- Dielectric Breakdown improvements in SiNx Split-2 imrpoving

Figures

- Contact Angle (and Refractive Index) for SiO2 and SiNx improvements



Milestone Summary (WP2.2.M2.2): Generic BB Improvements Threshold Current & Passivation – Integration Improvement

Author: Roel Daamen

Goals

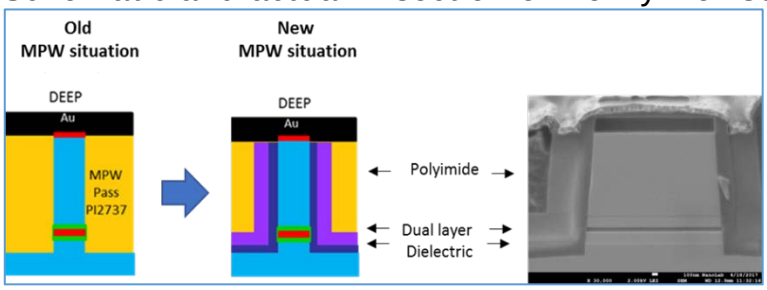
Improve the current MPW passivation to improve generic reliability (a.o. for lasers)

Achievements

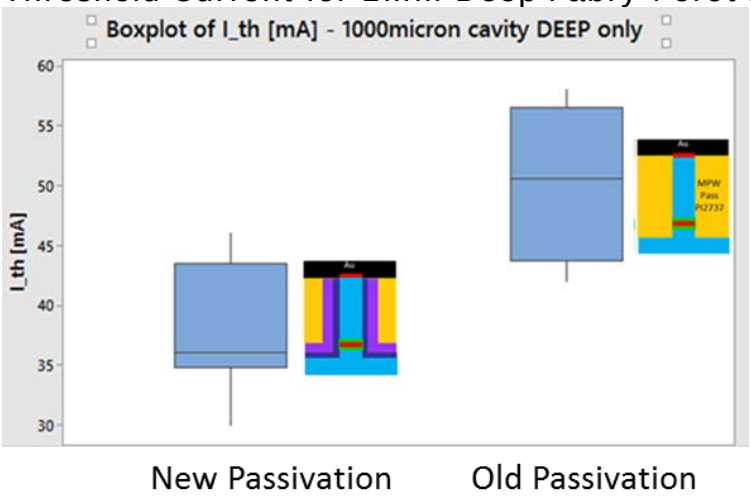
- New Passivation Integration approach identified and after several developments implemented on test wafers using Higher Quality Dielectrics (*see WP2.2-M2.1*)
- Dry etch recipes updated to better match existing Etch rates
- Excellent Laser Threshold currents were obtained in the deep sections where the Passivation is key.
- Excellent Reliability results obtained for the New Passivation
- New Passivation approach implemented on MPW SP19

Figures

- Schematic and actual X-section of Newly Devised Passivation



- Threshold Current for 1mm Deep Fabry-Perot Laser cavities



Work Package 3 – Building Block Improvement

Milestone Summary (WP3.1.M0): Technology and Design Concept – Modulator

Author: Weiming Yao

Goals

The goal is to outline concepts that will be pursuit for the high-speed modulator building block within this project and to indicate requirements on the technology platform.

Achievements

- We are planning to follow an iterative design approach for the modulator building block with 28, 56 and 112 Gbaud as target symbol rates.
- Relevant specifications are listed and given for the modulator BB to reach competitive performances.
- Based on literature study, speed limiting factors and design variants for high-speed modulators are presented and the CPW and segmented modulator electrode are chosen for this project to achieve the targeted performance.
- Initial requirements on the platform and in particular requirements on lithographic resolution are discussed. It can be concluded that the electrode geometry can be realized within the existing platform capabilities.
- The platform will need to transition to quantum well material and semi-insulating substrate in order to reach the targeted performance values.

Figures

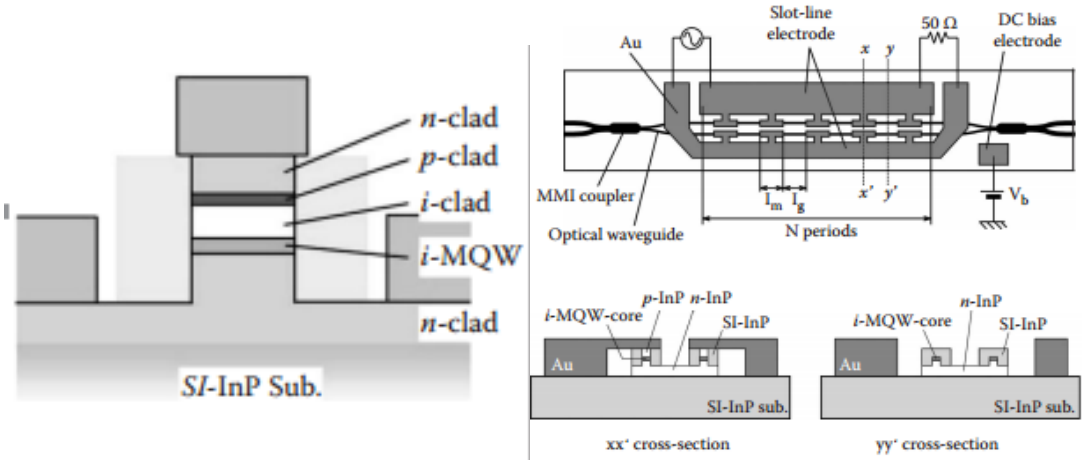


Figure 2: Concept for first and second iteration (left) designs (taken from Chen et al.). Segmented modulator structure for 80 GHz design (right, Akiyama et al.).

Milestone Summary (WP3.1.M0): Technology and Design Concept - RF Lines

Author: Weiming Yao

Goals

The goal is to finalize the concept that will be pursuit for the high-speed RF line building block within this project and to indicate requirements on the technology platform.

Achievements

- We decided to follow an iterative development procedure for the RF lines with incremental bandwidth increases from 20 GHz to 40 GHz and 80 GHz. Specifications on attenuation, length, impedance and return loss have been finalized.
- We investigated main factors that influence RF bandwidth and explored how these can be minimized through literature research and simulations. This led to the proposal of a novel RF line concept that is compatible to the generic platform.
- First details of the new concept have been established and its requirements on the platform technology have been discussed.
- The concept is illustrated in Fig. 1. A second level passivation layer using either polyimide or BCB acts as the dielectric material for the RF line building block. Via technology will be developed to connect the second level metal to the first level metal.
- This ensures low-loss transmission lines and adequate spatial separation of the RF field from the photonic layer.

Figures

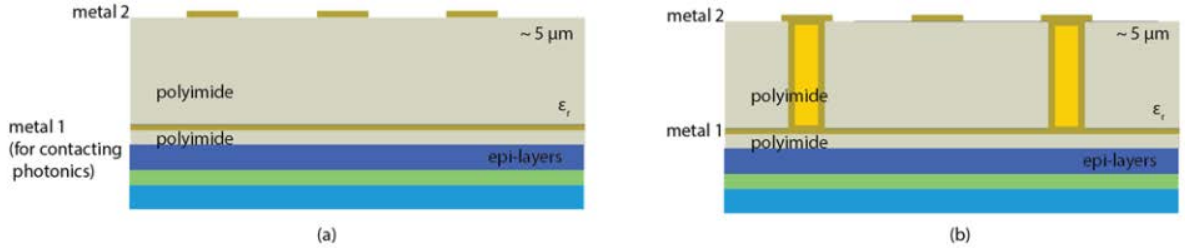


Figure 3: Desired cross section for the RF line building block. (a) Without via technology and (b) with via technology.

Report Summary (WP3.1.R0): Analysis and Design - Modulator

Author: Weiming Yao

Goals

This report details the analysis and design of the first iteration high-speed modulator, which has been taped-out in current multi-project fabrication runs for validation.

Achievements

- We detailed and motivated the need for incorporating multi quantum-well (MQW) material in the modulators in order to reduce drive voltage and therefore power consumption.
- MQW material growth and implementation in MPW runs is performed by Smart Photonics in close collaboration with Effect Photonics
- We analysed the influence of electro-plated metal on the modulator speed and performance. Skin-effect and resistive losses can be significantly reduced, motivating the use of thicker metal electrodes (Fig. 1).
- This is implemented since SP19 and its performance will be studied on modulators of SP20.
- Influence factors on modulator speed are analysed on the basis of a coplanar waveguide electrode configuration.
- Useful dimensions for the first iteration modulator design are synthesized for mask layout.

Figures

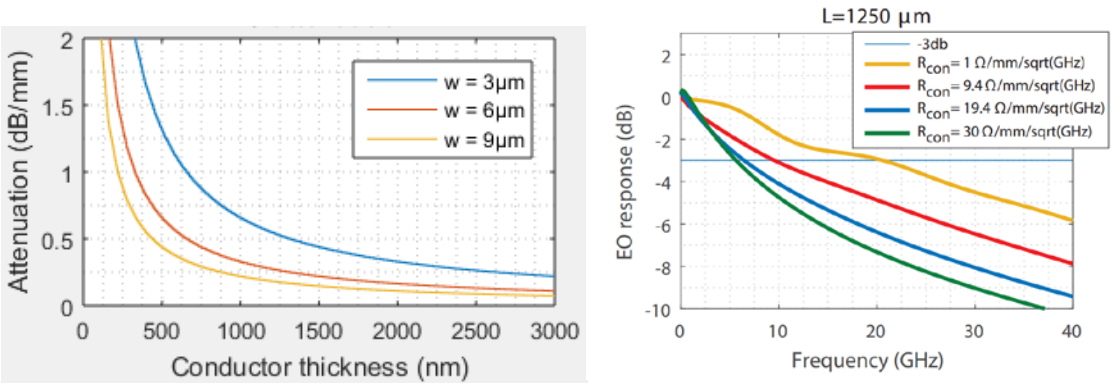


Figure 4: (a) Calculated microwave attenuation of modulator for varying electrode width and thicknesses. (b) Calculated EO response for varying modulator series resistance values.

Report Summary (WP3.1.R0): Analysis and Design – RF Line

Author: Weiming Yao

Goals

This report details the analysis and design of the first iteration broadband RF line component for routing high-speed signals on the photonic circuit.

Achievements

- We analysed the drawbacks of the existing RF line component design and indicated the main factors for achieving broadband operation. Major loss sources are doped p- and n- semiconductor layers that are neither ideal conductors nor dielectrics.
- Based on the insight, we propose a two-layer concept that overcomes the existing loss limitations through the insertion of a dielectric layer on top of the photonic circuit. Metal routing will be introduced on top of the latter dielectric layer.
- 3D electro-magnetic simulations are performed that confirm the broadband operation of the proposed RF line structure.
- The design is made compatible to the existing generic platform.
- Shielding planes are proposed that further promotes the separation of RF and optical functionality to guarantee low loss operation of both.
- Estimation of the bandwidth of the new structure yields >80 Ghz operation if length < 3 mm.

Figures

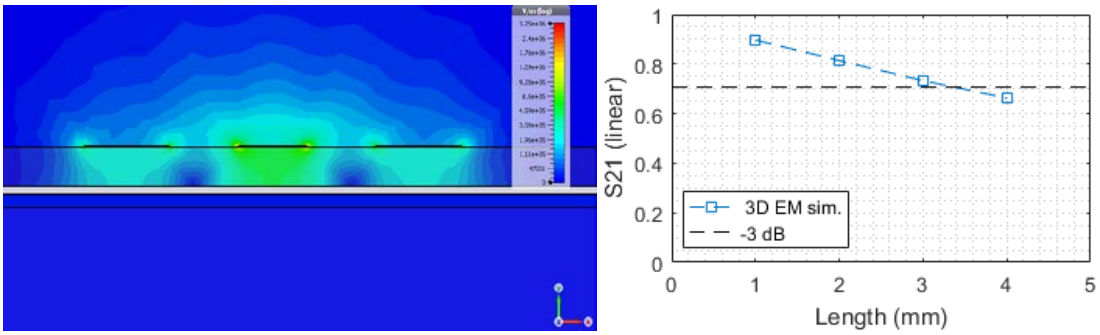


Figure 5: (left) Simulated E-field in RF CPW line. (right) S21 dependence on RF line length at 40 GHz.

Milestone Summary (WP3.1.M1): Mask Design Tape Out - Modulator

Author: Weiming Yao

Goals

The results from the analysis and design of the first iteration modulator building block are used to create the mask layout for the first design tape out.

Achievements

- We designed a range of modulator devices with varying geometric parameters around simulated optimum values and implemented them into mask layout.
- The designs were made to support high-speed on-chip probing for accurate device characterisation and testing.
- A new n-side contact and grounding scheme with n-metallization is accounted for.
- A test cell was filled with arrays of modulators, similar as shown in Fig. 1, so that both the electro-optic efficiency and EO bandwidth can be tested.
- In addition, microwave transmission line test structures have been designed that explore in more variation the electrode design space for the modulator component.
- The test cell has been released to SP20 which is based on a semi-insulating InP substrate and will be repeated in SP21 which in addition incorporates MQW material for lowering the drive voltage.

Figures

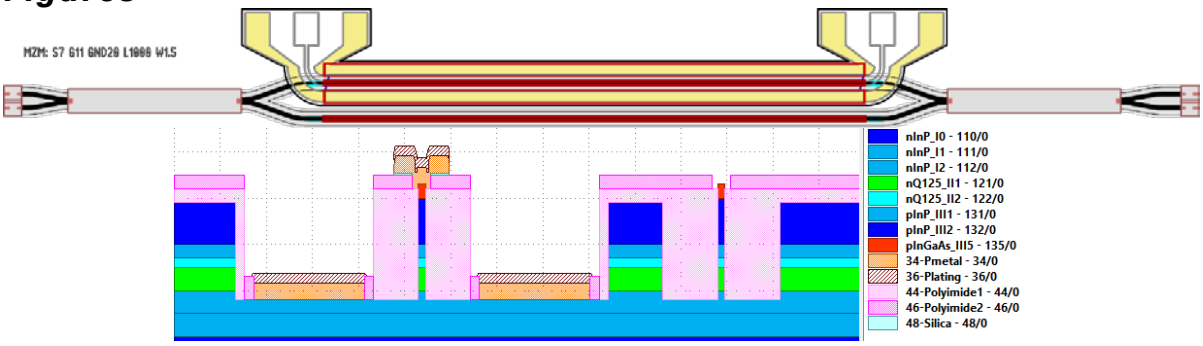


Figure 6: (top) Mask layout of single-drive traveling wave Mach-Zehnder modulator. (bottom) Cross section of CPW electrode design.

Milestone Summary (WP3.1.M1): Mask Design Tape Out – RF Line

Author: Weiming Yao

Goals

Test structures are to be designed that give more information on RF related material parameters of the platform in order to feed back into the high-speed component design.

Achievements

- We designed and implemented test structures for RF parameter extraction into run SP19. The designs will be repeated in subsequent MPW runs to track the evolution of RF parameters.
- Knowledge of material sheet and contact resistance to metal is important for RF line and modulator development. The circular transfer length test structure is very suitable to extract both and has been implemented in mask layout (Fig. 1 left) for varying underlying layer compositions.
- The metal series resistance is an important parameter that determines RF loss and can be extracted from Van Der Pauw measurements on structures shown in Fig. 1 center.
- The series resistance at DC and high frequencies can be measured from the structures shown in Fig. 1 right. RF transmission lines can be characterized and the obtained S-Parameters can be used to fit a general RLGC model in order to determine the R component.

Figures

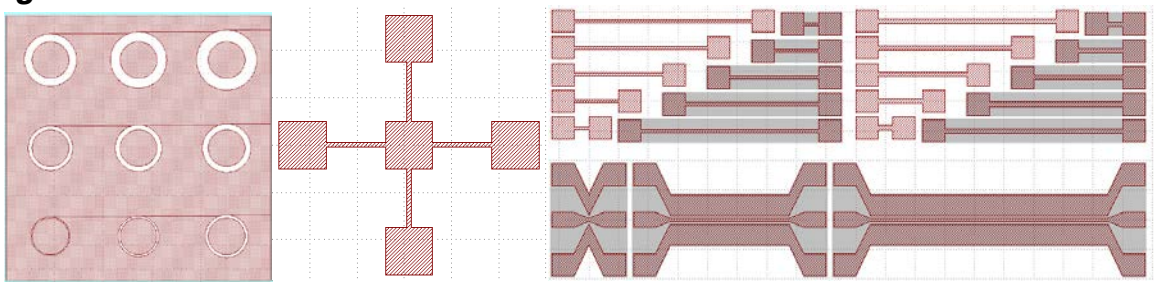


Figure 7: (left) Circular transfer length measurement structures for sheet and contact resistance extraction. (center) Van-der-Pauw sheet resistance measurement structures. (right) Series resistance extraction from DC and RF transmission line measurement.

Milestone Summary (WP3.2.M0): Report on the current state of the PDK and issues list

Authors: Rui Santos

Goals

This report describes the status of the SMART Photonics MPW PDK. This includes an overview of the design manual, building blocks and design rules is made.

Achievements

- Description of the state of the art of the SMART Photonics PDK
- Description of the improvements to be added to the PDK
  - Extended version of the DRC.
  - Experimental data of BB.
  - Inclusion of new BB to the PDK.

Current status of the SMART Photonics PDK

A Process Design Kit (PDK) is a collection of foundry-specific data files and script files used in a specific chip design flow. A PDK's main components are models, symbols, technology files, parameterized cells, and rule files. The PDK is mostly, but not entirely, described in the design manual from the foundry.

Currently the SMART Photonics MPW PDK is described in the design manual version 0.3 released November 4th 2016 (**Error! Reference source not found.**). The PDK is now implemented in the mask layout software PhoeniX OptoDesigner.

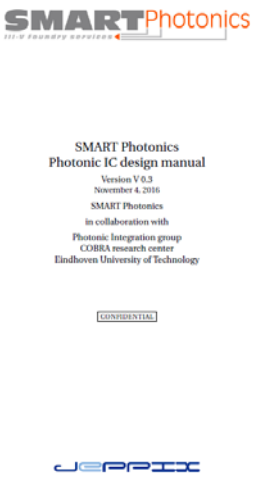


Figure 8: SMART Photonics manual.

Milestone Summary (WP3.2.M1): Figure of Merit for the building blocks from MPW SMART PDK

Authors: Rui Santos

Goals

This report identifies the figures of merit (FoM) of all the building blocks available in the SMART Photonics MPW PDK. The objective is to identify the key parameters that will enable setting performance specifications.

Achievements

- Definition of the FoM of the building blocks.

Figure of Merit for the Building Blocks

The Figure of Merit (FoM) is the identification of the main performance characteristic that will be used for validation of the performance of each individual building block (BB). In the following table a list of the BB with the corresponding FoM, including the measurements units, is shown.

SMART PHOTONICS Building Blocks

Type	Name	FoM	units
passive	Shallow waveguide	waveguide loss	dB/cm
passive	Deep Waveguides	waveguide loss	dB/cm
passive	Shallow curve	excess loss	dB/90°
passive	Deep curve	excess loss	dB/90°
passive	Linear Taper	insertion loss	dB
passive	Parabolic Taper	insertion loss	dB
passive	MMI coupler 1x1	insertion loss	dB
passive	MMI coupler 1x2 Shallow	split ratio	dB
passive	MMI coupler 1x2 Deep	split ratio	dB
passive	MMI coupler 1x2 Low Reflec	split ratio	dB
passive	MMI coupler 2x2 Shallow	split ratio	dB
passive	MMI coupler 2x2 Deep	split ratio	dB
passive	MMI coupler 2x2 8515 Shallow	split ratio	dB
passive	MMI coupler 2x2 8515 Deep	split ratio	dB
passive	MMI coupler 2x2 7228 Shallow	split ratio	dB
passive	MMI coupler 2x2 7228 Deep	split ratio	dB
passive	Shallow Deep transition	insertion loss	dB
passive	waveguide crossing shallow	insertion loss	dB
passive	waveguide crossing deep	insertion loss	dB
passive	isolation section shallow	electrical resistance	Ω
passive	isolation section deep	electrical resistance	Ω
active	Phase Modulator (EOPM) shallow	EO efficiency	°/V.mm
active	Phase Modulator (EOPM) deep	EO efficiency	°/V.mm
active	Phase Modulator (EOPM) RF	EO efficiency	°/V.mm
active	SOA	gain@current density	dB/cm(nm) @kA/cm^2
active	PIN diode	responsivity	A/W
active	Saturable absorber	absorption	A/W
passive	DBR	wavelength	nm

Milestone Summary (WP3.2.M2): Definition of Composite BB Figure of Merits

Author: Weiming Yao

Goals

To improve on the PDK and design manual, not only basic building blocks (BBBs) but also more complex, composite building blocks (CBBs) need to be well characterized. We define here the most relevant figure of merits for the existing CBBs.

Achievements

- We consolidated the collection of composite building blocks from recent R&D developments on the generic integration platform.
- We defined the basic figure of merits (FoM) for the developed composite building blocks, listed below:
  - Coupled-cavity tuneable laser
  - Coupled-cavity tuneable laser extended tuning range
  - Widely tuneable laser with MZI filter
  - EAM modulator
  - MZM modulator
  - Mode locked ring laser
  - Mode locked linear laser
  - DBR laser
- Initial concepts for extracting these FoMs have been drafted and can be implemented in future CBB test cells.
- This contributes to standardization and tracking of the composite building blocks.

Figures

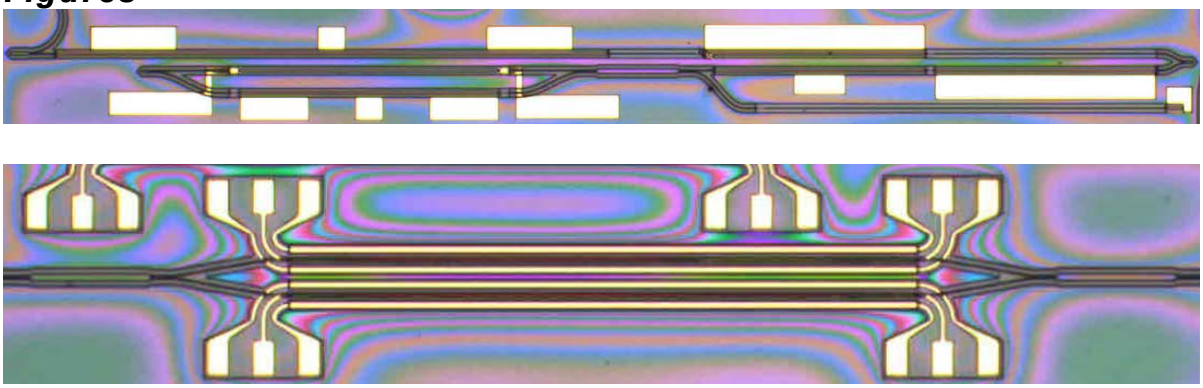


Figure 9: (Top) Microphotograph of coupled-cavity laser and (bottom) picture of Mach-Zehnder modulator.

Report Summary (WP3.2.R0): Definition of Measurement Procedures

Author: Weiming Yao

Goals

Test structures have been designed to extract the figure of merits of each basic building blocks on the platform. For each test structure, this item defines the specific measurement procedures that needs to be performed in an automated manner.

Achievements

- Based on previous expertise we defined electrical test structures for extracting figure or merits (FoM) for the basic building blocks (BBBs) of the platform. These test structures can be probed electrically and therefore support on-wafer automated measurements (Test Cell 2).
- Fiber alignment is still needed for the majority of pure optical FoMs such as reflection or transmission values of passive components and its measurement procedure has been specified in detail (Test Cell 1).
- A quasi-standard description is being developed for specifying the measurement procedure incorporating the source and sense conditions and pin positions of the test cell.

Tables

Table1: List of test structures in BB Test cells for SP20

Test Cell 1	Test Cell 2
Insertion Loss EOPM	Spectral gain structure
Insertion Loss Metal on top of WG	SOA gain, saturation structure
MMI insertion loss	EOPM efficiency
MMI reflections	Current injection phase efficiency
MIR reflections	MMI imbalance, electrical + optical
WG crossing reflection	Ring resonator loss measurement
Shallow-Deep transition reflections	PIN PD responsivity
Shallow-Deep transition insertion loss	CD SEM for WG opening
Isolation section insertion loss	
WG cross insertion loss	
MMI imbalance	

Report Summary (WP3.3.R0): Design of Standard MPW Building Block Test Cell

Author: Weiming Yao

Goals

Standard building blocks need improved characterization of their figure of merits, yielding values that will be tracked along different fabrication runs. This characterization should be performed in an automated way on wafer and on die from building block test cells. This item describes the design of those test cells for automated measurements.

Achievements

- We created test structures for all basic building blocks offered in the platform and taped them out into two test cells (Fig. 1).
- Test cell 1 is aimed at optical component characterization, mainly for passive devices. In particular, splitting ratio, insertion loss and back reflection levels are to be measured through Fabry-Perot and OFDR measurement techniques.
- Active and EO-components are placed on cell design 2 for on-wafer and on-die automated measurements involving probe cards.
- The electrical pad layout follows quasi-standards from the running European PixApp project, tackling generic packaging solutions. This enables efficient and fast measurement of the main device parameters in the electrical domain without accessing the optical signals and enables on-wafer measurements.
- Test cells are prepared for top side n-contact as well.

Figures

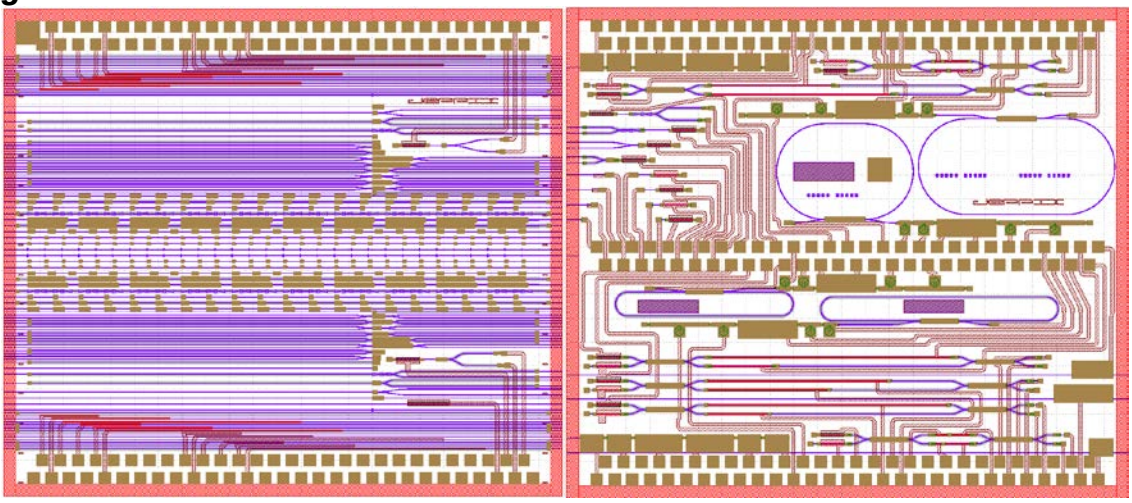


Figure 10: (left) Test cell 1 for optical component testing and (right) test cell 2 for automated electrical component testing.

Milestone Summary (WP3.4.PDA.M0): Development of PDAFlow Template

Authors: Marcel van der Vliet

Revisions

Version 0, 19 Jun 2017, Marcel van der Vliet, Initial document

Introduction

This document discusses the status of the PDAFlow template

PDAFlow Template

The PDAFlow template is created and documented in 'PHX-0112 PDAFlow PDAFoundry Manual.pdf' dated 9 February 2017. This document describes the procedure to add building blocks to an PDAFlow compliant PDK.

Chapter 11: 'Combining the pieces' Explains how you can start from scratch creating your own PDK. This chapter is supported with a number of spt and cc files that provide a template. This should be sufficient information to start adding Building Blocks to an existing PDK.

Conclusions

The first draft of an PDAFlow Template is supplied, and this should enable the TU/e to start adding building blocks to PDKs.

Figures

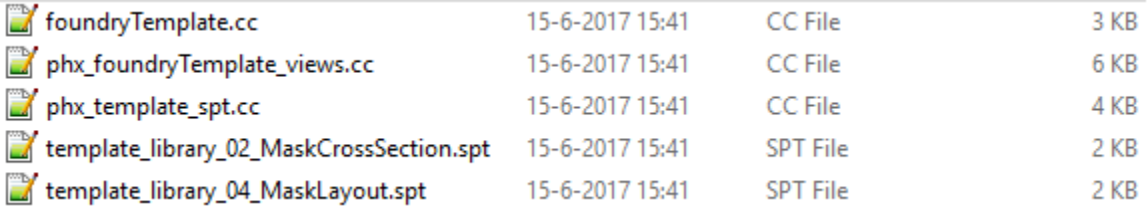


Figure 11: List of spt and cc files that provide a template..

Report Summary (WP3.5.R0): 400G transmitter concept

Author: Saeed Tahvili

Goals

The goal is to propose 400G transmitter concept as the project demonstrator. Two essential building blocks which are going to be developed in this project are integrated tunable lasers and fast modulators.

Achievements

- IEEE has identified the next generation standard as 400 Gb Ethernet (400 GbE) (Figure 1.a). We decided to set a concept 400G transmitter as the project demonstrator.
- We investigated several possibilities depending on the number of (integrated) optical lanes and line rates, i.e. 16λx25Gbps, 8λx50Gbps, and 4λx100Gbps. The 8λx50Gbps option (Figure 1.b) is the most interesting option in terms of level of integration and line rate.
- Two flavours of the proposed 400G transmitter are 8 λ lanes integrated with either 25GBaud modulators under PAM-4 modulation, or 50G bandwidth optical modulators.

Figures

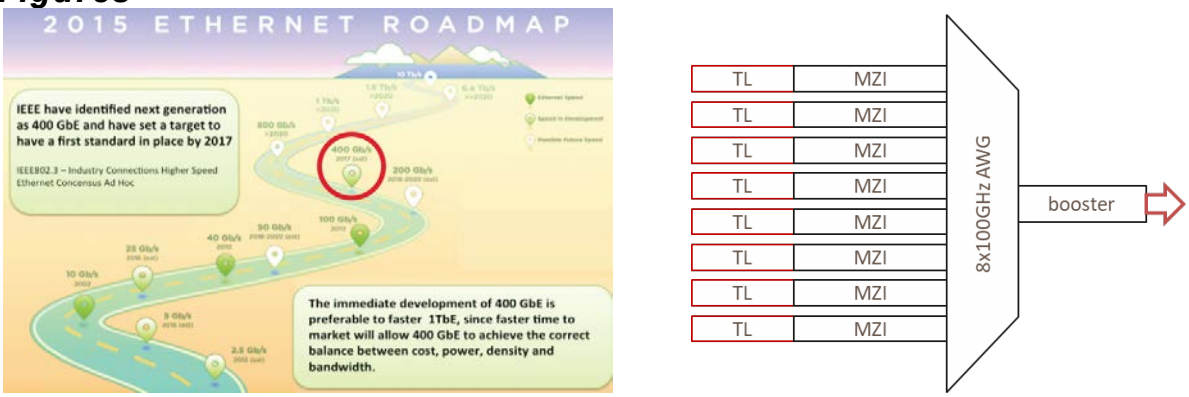


Figure 12: (a) Ethernet Alliance 2015 roadmap (b) 8x50Gbps (PAM-4) DWDM transmitter concept. TL: tunable laser, MZI: mach-zehnder modulator

Report Summary (WP3.5.R1): Demonstrator Sensing

Authors: Michael Haverdings

Goals

The goal is to propose a chip architecture specifically for a sensing application based on an existing product line.

Achievements

- The optical power budget relates directly to a performance improvement
- Polarization behaviour in AWG contributes to the stability of the sensing measurement. Not only in the main transmission peaks, but also in the side-lobe behaviour. On chip-polarization crosstalk is considered as a realistic source of instability. In addition, fabrication tolerances lead to polarization dependent behaviour.
- Improving the building blocks will increase the current sensing performance, setting aside potential architecture improvements. To demonstrate the performance improvement, we propose a basic AWG design with SSC.
- AWG target: side-lobe suppression at least 25 dB in wavelength range of 1500-1600 nm. IL of max -3 dB. Number of channels at least 48. Channel spacing of 200 GHz or lower (up to 50 GHz). Polarization dispersion of less than 1 pm on central channel wavelength.
- SSC target: IL of max -2 dB from fibre to chip, over a wavelength range of 1500-1600 nm. Polarization dependency of less than 0.5 dB

Figures

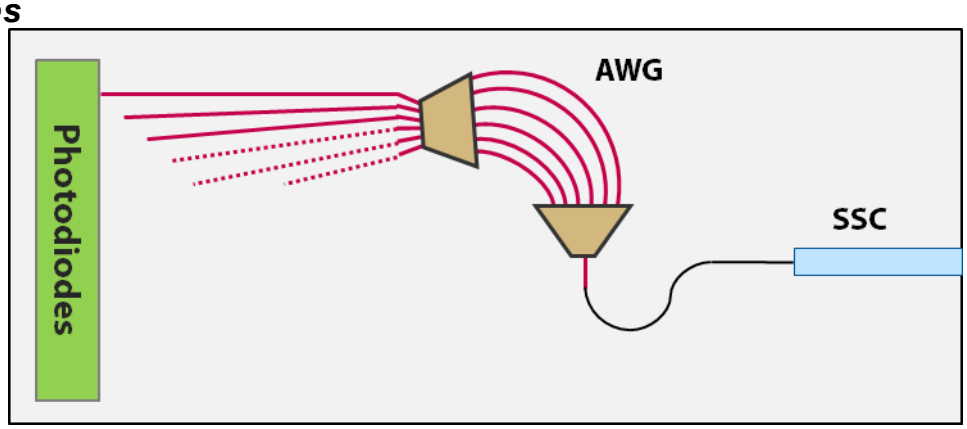


Figure 13: Basic AWG concept design to demonstrate improved sensing by having improved BB's.

Work Package 4 – Process Improvement

Milestone Summary (WP4.M1.1): Specific tasks and milestones defined; WP started. (WP4.M1.2): Quantifiable criteria for each milestone defined

Author: Longfei Shen

Goals

The goal is to obtain an overall planning for this work package at the starting phase of the project. The planning should be made by means of a milestone list with quantifiable criteria which can be used for reviewing the progress of this project in a later stage.

Achievements

- We have planned to start with five parallel tasks in this work package, and each of them has been arranged with a task lead.
- Each task contains three milestone points and one final report. Attention has been paid to the synchronization between these milestones and the MPW run schedule that is defined in WP 2.
- Quantifiable criteria has been made for each milestone point. They are defined according to the specifications of building blocks and device demonstrators (outputs from WP 3).
- The samples and characterization methods are also proposed to for the experimental verification of these criteria.

Figures

Tasks	**M**ilestones / **D**eliverables		Responsible	Due date
T 1. General planning	M 1.1	Specific tasks and milestones defined; WP started	Longfei	Dec-16
	M 1.2	Quantifiable criteria for each milestone defined	Longfei	Mar-17
T 2. Al-MQW based modulators	M 2.1	Designed MQW characterized, shallow-etch modulators demonstrated	Longfei	Dec-17
	M 2.2	Etching and passivation processes developed: ready for MPW validation	Longfei	Jun-18
	M 2.3	Modulator validated in MPW: ready for release	Rob	Mar-19
	D 2.4	Report on process optimization and insights for 100 Gbps modulators	Longfei	Jun-19
T 3. Zn-diffusion based A/P integration	M 3.1	Zn-diffusion time determined: ready for joint MPW validation	Rene	Jun-17
	M 3.2	Zn-diffusion process validated in joint MPW: ready for transfer to Smart	Rene	Mar-18
	M 3.3	Zn-diffusion process transferred and validated in MPW: ready for release	Rob	Dec-18
	D 3.4	Report on process integration and device characterization	Longfei	Dec-18
T 4. Thick insulation and RF lines	M 4.1	BCB insulation and metal plating tested: ready for joint MPW validation	Tjibbe	Sep-17
	M 4.2	Process validated in joint MPW (post-processing): ready for transfer	Tjibbe	Mar-18
	M 4.3	Process transferred and validated in MPW: ready for release	Rob	Sep-18
	D 4.4	Report on process integration, insights for 100 Gbps RF lines	Longfei	Dec-18
T 5. DUV lithography and etching optimization	M 5.1	DUV lithography introduced to MPW	Rob	Jun-17
	M 5.2	Etching process optimized, ready for transfer to MPW	Longfei	Mar-18
	M 5.3	DUV lithography introduced to Triplex platform	Joost	Jan-19
	D 5.4	Report on process integration (lithography and etching) in MPW	Rob	Jan-19
T 6. Stepper lithography integration	M 6.1	Process developed for AZ and MaN based lithography	Robert	Aug-17
	M 6.2	Overlay tested and optimized	Robert	Jan-18
	M 6.3	Process introduced to Smart MPW	Rob	Sep-18
	D 6.4	Report on process integration, insights for fabricating new BBs	Longfei	Dec-18

Figure 14: Overview of the milestone list of WP4.

Milestone Summary (WP4.M3.1): Zn-diffusion time determined: ready for joint MPW validation

Author: Longfei Shen, Rene van Veldhoven

Goals

The goal is to perform Zn diffusion in epitaxial layers and characterize the diffusion rate at different conditions. The results will be used in the design of experiments with MPW wafers and processes.

Achievements

- We have performed successfully the Zn diffusion in a new reactor and measured the doping concentration.
- The diffusion profiles in various materials are measured at different temperatures. The diffusion rate coefficients are determined from these profiles.
- The surface quality of Zn-diffused samples covered by a SiNx mask layer has been inspected, to select the optimal process conditions.
- Zn-diffusion in MPW wafers have also been observed. A more accurate empirical model at the selected process conditions will be determined with more data points in the next stage of this task.

Figures

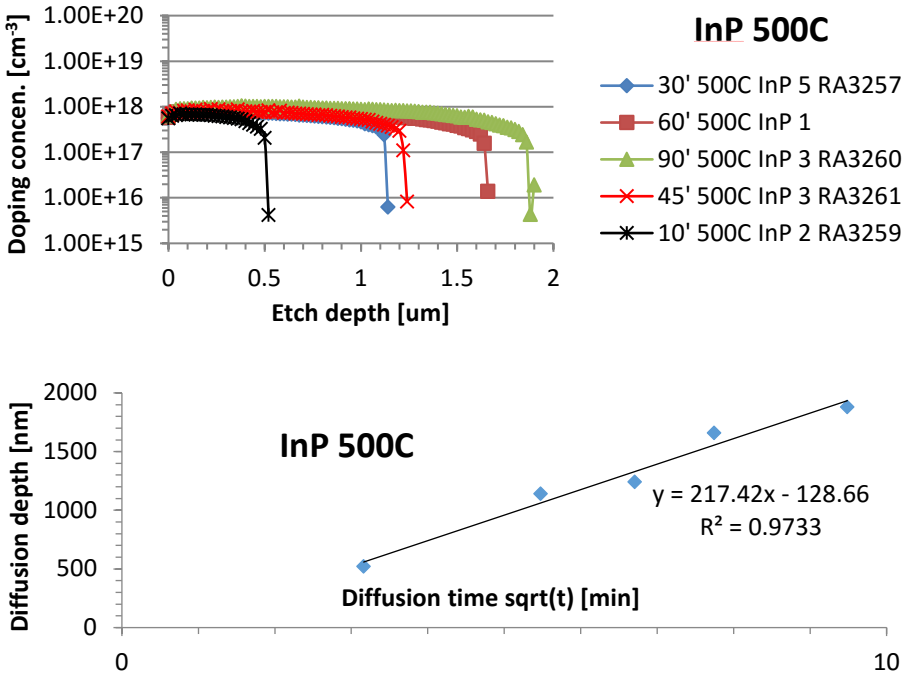


Figure 15: Overview of the milestone list of WP4.

Milestone Summary (WP4-M5.1): DUV lithography introduced to MPW

Author: Roel Daamen, Erik den Haan

Goals

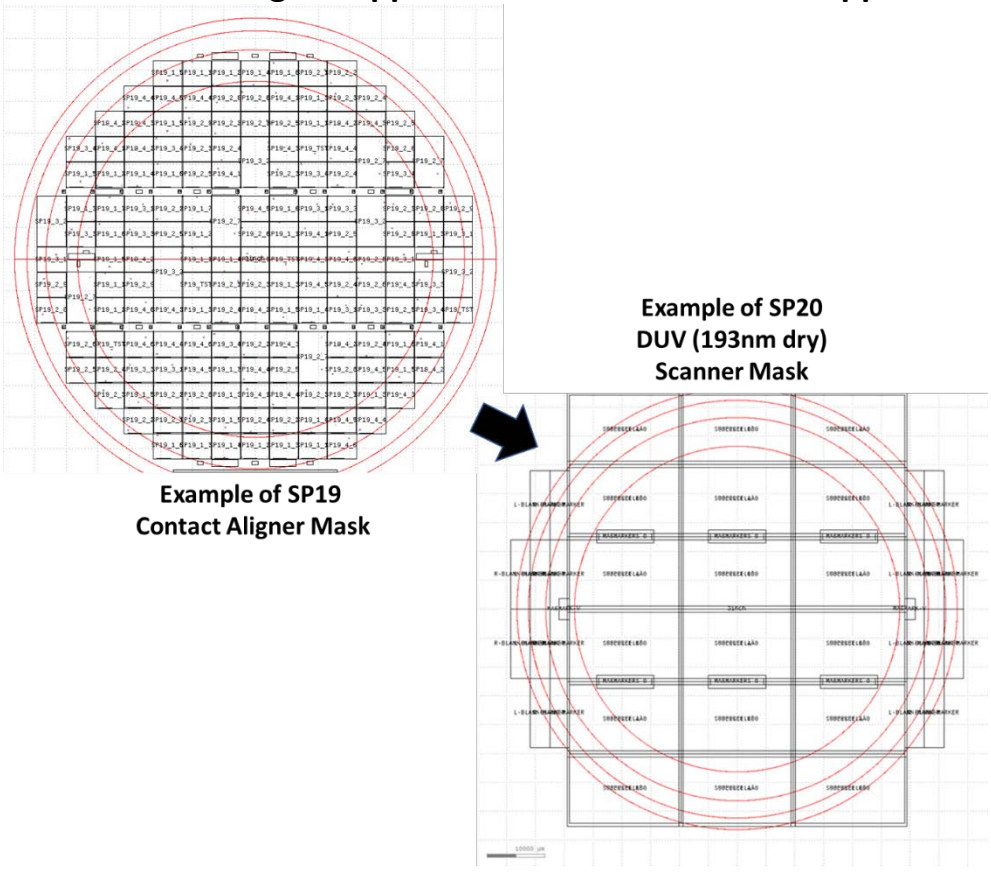
Introduce DUV (193nm dry) lithography in the MPW flow, starting from the SP20 run of June 2017

Achievements

- For the DUV approach so-called super cells have been created, which fit 12 MPW cells of 4x4.6mm. A single supercell can be replicated 18 times on a 3 inch wafer.
- DUV mask design approach implemented on SP20, containing 2 supercells each with 9-fold replication.

Figures

- **Contact Aligner Approach versus DUV scanner approach**



Partners

Open Innovation Photonic ICs

OpenPICs

Technical Summary Brief

(07/2017 – 12/2017)

Europese Unie

Europees Fonds voor Regionale Ontwikkeling
Europees Innovatieprogramma Zuid-Nederland

Photonic Integration Technology Centre

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Introduction

The Open Innovation Photonic IC project (OpenPICs) has the goal to improve and mature photonic integration technology and widen its adoption by focusing work on four different domains: market demands, process characterization, building block improvement and process improvement. Significant work has been performed during the first reporting period (09-2016-06/2017) where the focus lied on initiating the project and establishing concepts and fundamentals in all four domains. In this reporting period, we have carried on the work along the main established lines, leading to incremental results in each domain. The following technical brief will shortly report the main achievements of this reporting period.

Work Package 1 – Market Demands

Milestone (WP1.M4): Key Performance Indicators for MPW runs (KPIs)

Summary

Open access technology platforms exist as a solution for PIC prototyping on a fab-less lab-less model. They provide cheap fabrication entry costs and relatively simple chip design process for first entry designers. They target public and private sector for SMEs and big companies. The ecosystem surrounding open access technology platforms include research, design, software tools and foundries. Foundries are a critical module within the ecosystem since they develop the technology for the platforms to fabricate the chips. Therefore, the MPW runs need to comply with several KPIs in order to be competitive as a PIC entry fabrication service. Those KPIs have been described. KPIs from service point of view:

- Number of leads resulting in a MPW run
- Designs per MPW run vs available cells and cumulative per year
- Price per mm^2 / wafer size
- Delivery time

KPIs from the technical point of view:

- Components performance per foundry
- Testing cells
- Packaging templates available
- Software tools available

Work Package 2 – Process Characterisation

Milestone Summary (WP2.2-M3.1): Generic BB Improvements Planarisation Sequence on SP20

Goals

Improve robustness by changing/switching the Polyimide Sequence to ensure a smoother step for the Metallization (especially taking into account Semi-Insulating substrate offerings).

Achievements

The Polyimide order has been switched *from:* SP19: PI1→PI2 *to* SP20: PI2 *Contact* →PI1 *Planarisation*.

Basic 1mm All Active laser parameters on MPW SP20A are equal to or better than SP19.

SP20A Threshold Current 22.8mA/mm, Series Resistance ±3 Ohm and Slope Efficiency of 14.5%

Milestone Summary (WP2.3.-M1.1): NEW Building Block Introduction DBR laser

Goals

Introduce a DBR laser Building Block in the MPW flow.

Achievements

A tunable DBR laser with excellent performance has been implemented in SP19

- Threshold Current ±20mA
- High Output Power up to ±11mW
- Single Mode operation with SMSR > 50dB

DBR quality is good enough for creation of a Building Block and implementation into the PDK.

Work Package 3 – Building Block Improvement

Report Summary (WP3.3.R1): Design of Composite BB Test Cell

Goals

We designed a test cell containing the most recently developed composite building blocks to quantify and extract the most common characteristics.

Achievements

- We collected the recently developed cBBs including a widely tunable laser, a compact coupled-cavity laser, a Mach-Zehnder modulator, a DBR laser and an electro-absorption modulator.
- We standardized their dimensions and parameters so that the same building blocks can be used in a custom component library.
- The test cell is compatible with the standard testing pad layout to support automated measurements.

Report Summary (WP3.4.PDA.R0): Full Documentation of PDAFlow Template

Summary

A complete documentation in form of a 13 chapter long document has been created that holds the necessary code examples to work with PDAFlow. The document describes in detail how PDKs can be created and building blocks can be added to the PDAFlow environment. It ends

with aspects on how to connect the different code pieces and how a working example can be compiled. It also describes how the interface to the foundry looks like and which design aspects during coding needs to be considered.
The document is available to the members of the PDAFlow foundation, that targets to work towards a combined photonic design solution.

Milestone Summary (WP3.4.DRC.M0): DRC Implementation in PDKs

Summary

A DRC deck is implemented and documented for the Smart PDK September 14 Release 5.1.4 version. The following DRCs are implemented in the SMART Photonics PDK.

- All the design rules mentioned in SMART Photonics design manual are implemented in the SMART Photonics PDK except the rule ISO.0.1 is not implemented, whereas the length of cbIsolation is required to be larger than 10.0 um.
- For ``WG.0.2|0.3|0.4``, additional warning for DFM values can be switched on by define "WG_WARNING_SMART".
- DRC of ``WG.0.7|0.8`` is only enabled by defining "EXTRA_DRC_SMART".
- DRC for ``bounding boxs overlapped`` is enabled to check if cells with bounding boxs overlap with each other or not.
- DRC for ``Waveguide/text too close to the building block outline`` is enabled to check if there is minimum space between waveguide or text to the building block outlines.

Report Summary (WP3.4.DF.R0): Design Flow Document

Summary

This document describes the design flow from general idea to actual PICs (Photonic Integrated Circuits). First, there is not ONE design flow that fits all. Dependent on the application different design flows are used. On top of that, through time, there is an evolution of the design flow. This document will have the view that the Photonic Design Automation (PDA) design flow evolution will follow a similar evolution as of the Electronic Design Automation (EDA) design flow. The document will be used to identify the areas for improvement for the PDA design flow. It is also recognized that in many aspects the PDA design flow will have its own challenges unknown to the EDA design flow.

Work Package 4 – Process Improvement

Milestone (WP4.M5.1): AZ resist process development on PAS 2500/40 stepper

Summary

In this report the optimal exposure settings of AZ resist used on a PAS 2500/40 stepper has been presented. In the current generic process to produce optical chips we still make use of contact exposure. Because of the contact between mask and wafer this technique is sensitive to defects (damaged wafers and mask wear). From a production point of view one would rather use projection exposure as it is a contactless way of exposing optical resist. Particles or defects that are present on the mask will be reduced in size on wafer level and there is hardly any mask wear. The available tool in the NanoLab@TU/e cleanroom for projection exposure is the PAS

2500/40 Stepper from ASML and the resist of choice for process development on this tool is AZ4533.

Based on the FEM experiments performed on the AZ4533 resist with the PAS 2500/40 stepper the optimal exposure energy is set to 400mJ and the optimal focus depth is set to -1 micron. Based on these settings, wafer critical dimension uniformity measurements show the following values based on 246 measurements: the values are respectively 1531nm (+/-64nm) for top and 1579 (+/-68nm) for bottom. The loss of width, because of overexposure, needs to be taken into account at mask design level.

Outlook

The plan for the next reporting period will be briefly outlined here. With respect to meeting market demands, we will focus on creating a roadmap that will help aligning better the technical developments with actual market requirements. On the process characterization side measures that increase process maturity will be implemented such as tiling and novel passivation schemes. In addition new process building blocks such as semi-insulating substrate or more effective EO materials will be made available. First results will also be available for the novel building blocks and significant improvements will be done on the design environment. Furthermore, Technobis and Effect Photonics are working on the demonstrator designs and finally multiple highlights in the area of process development such as processes for high-speed RF lines and AI-based modulators will be released.

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Technical Summary Brief

(01/2018 – 07/2018)

Europese Unie

Europees Fonds voor Regionale Ontwikkeling
Europees Innovatieprogramma Zuid-Nederland

Photonic Integration Technology Centre

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Introduction

This summary brief will give an overview of the activities carried out in the first half of 2018 within the Open Innovation Photonic IC project. The activities are divided between four work packages: Market Demand, Process Characterization, Building Block Improvement and Process Improvement. Significant progress has been made in WP1 through the release of a platform roadmap, defining the state-of-the-art of open access generic photonic integration platforms based on InP and SiNx, and presenting the technology projections for the coming 2-5 years. It has been distributed in three major conferences this year already. In addition, key performance indicators of the multi-project wafer runs (MPW) have been gathered to better understand the operational aspects of the open access runs. More than 100 designs have been prototyped alone in the last two years. In WP2, the Smart Photonics foundry has made progress in implementing characterization and monitoring methods so that the pilot manufacturing line performance and stability can be accurately tracked. This will help in achieving reproducible wafers and devices. Metrics such as laser threshold current, series resistance are being tracked in addition to optical loss and waveguide dimensions. In WP3, steady work on building block development has been performed, e.g. the fabrication of DBR laser modules with several mW output power and the demonstration of fast optical modulators exceeding 20 Gb/s. In addition, building block test structures for PDK data generation have been revised and periodically added to MPW runs. In WP4, an interesting process to fabricate low-loss optical waveguides has been trialled and investigated in-depth, yielding useful insight to future process improvements. More details on the activities in each WP are given below.

Work Package 1 – Market Demands

Milestone Summary (WP1.M3): Platform Roadmap

This initiative was coordinated by JePPIX and driven by all the partners of the JePPIX open access technology platforms in InP and SiNx. It represents the current development of such technologies, reports the market analysis of photonics integration, shows the analysis of each part of the value chain on the ecosystem and the projections on new technology nodes for photonic integration technology.

The 2018 roadmap synthesizes JePPIX's analysis of the PIC market and market requirements for the coming 2-5 year timescale. Important technology developments required to foster the foreseen market growth are analysed in many areas, including fabrication processes and equipment, design software, packaging and testing.

As part of the dissemination activities of WP1, a publicity campaign was performed to disseminate the JePPIX roadmap 2018. The campaign included:

- Release of a bulletin https://mailchi.mp/a47397a9c0b9/jeppix-bulletin-april-2018 (369 opens)
- 100 USB stick with the roadmap distributed at OFC 2018
- Announcement in LinkedIn (49 likes, 266 views), e-broadcast (>400 people)
- JEPPIX webpage with link to download (980 views, 249 downloads)

http://www.jeppix.eu/vision/

- Interview in Photon Delta website (1797 views) https://www.photondelta.eu/news/insights/jeppix-launches-2018-roadmap-at-ofc/#sthash.875UzhSc.dpbs
- WTMF copies of Roadmap (50 copies)
- IPRM/CSW Boston (20 copies)

Milestone Summary (WP1.M4): Key Performance Indicators for MPW Runs (KPIs)

Open access technology platforms exist as a solution for PIC prototyping on a fab-less lab-less model. They provide cheap fabrication entry costs and a relatively simple chip design process for first entry designers. The value of MPW runs translates into innovative application fields and improvement of performance of the current building blocks. In order to retrieve valuable information to analyse and overcome KPIs challenges valorisation methods are needed. Within WP1 different approaches to gather crucial information on the technology have been implemented. First in order to bridge the gap between technology development and commercially available products we have generated several reports “linking BB to products”. In this way we are able to analyse both, the real necessities of a company to create a prototype and the needs of the current photonic components to perform as required by the industry.

Another approach we took is gathering valuable information from previous MPW run users both from the public and private sector. This action allows us to evaluate the performance of the complete value chain of open access technology platforms and offer the required information to run the adequate root-cause methodology in each part of the value chain (administrative process, BB development & performance, software, design and packaging). The results of this analysis are fed back to each part of the ecosystem.

The activities of WP1 during the first half of 2018 focused on 2 parts: one, the methodology of acquiring clients, where we have been tracking the procedure of acquiring or starting new projects that lead to an MPW run. This activity aims to increase the number of effective leads and to provide broad dissemination and feasibility support for PICs to first entrance users in different application fields. Second, since August 2017 we worked on creating the JePPIX roadmap 2018. This roadmap is a breakpoint in the technology development and represents the photonic integration ecosystem. This roadmap serves as a guideline to the PIC market; moreover, JePPIX members are also contributing to the AIM road mapping initiative led by MIT and the World Roadmap for Integrated Photonics, led by Photon Delta.

Work Package 2 – Process Characterization

Milestone Summary (WP2.1-M1.3): Generic MPW Data - Update June’18

Goals

Improve stability of the Equipment and Processes as used in the MPW.

Achievements

Stability improvements have been introduced throughout the Smart Photonics line. The introduction of the Passivation and Polyimide improvements in SP19 and SP20 have resulted in a further reduction of Threshold Currents in SP21 to below 25mA/mm for All Active FP lasers.
The epitaxy department has introduced a higher number of calibration runs that guarantee a much more controlled PL on released wafers.
And the MPW introduction of 193nm Scanner lithography has made a large improvement on Waveguide Line Width control. Standard deviations for Waveguides have been reduced from circa 6% to below 1% (1sigma).

Note on Milestone WP2.2-M2.2 Dummy Structures / Tiling

The implementation of Dummy Structures and Tiling Density has been delayed to MPW SP24B for the July 2018 Tape-Out

Milestone Summary (WP2.3.-M1.2): Semi-Insulating Substrate

Goals

Verify basic MPW performance when using Semi-Insulating substrates in the MPW B-runs.

Achievements

Performance parameters for Semi-Insulating (SI) substrates were similar to the standard MPW process parameters on S-doped InP. Deep waveguide losses below 3dB/cm and laser threshold currents below 25mA/mm with 0.15 slope efficiency have been measured. As expected, only a slight increase of the series resistance of almost 3 Ohms has been observed. Offering SI-substrates and processing is therefore considered to be low risk.

Work Package 3 – Building Block Improvement

Milestone Summary (WP3.1.M0): Technology and Design Concept - Laser

In this milestone we present specifications of the tuneable lasers defined by Technobis for use in their demonstrator. We examine different tuneable laser geometries and present their state-of-the-art properties. The specifications of these lasers define the required technology. We consider the Indium Phosphide (InP) technology platform provided by Smart Photonics and the silicon nitride (SiN) technology platform provided by Lionix International (TriPleX) for development of the low linewidth laser.

Report Summary (WP3.1.R0): Mask Design Tape-out, Analysis and Design - Laser

In this document we presented design considerations for the DBR test structures and DBR-based tuneable lasers. In order to use DBR gratings in various systems (lasers, filters or others) designers should be able to predict the performance of gratings using theoretical models. A prerequisite to accomplish this is that the behaviour of the gratings for different geometries (pitch, length and strength) should be properly characterized. A next step is to compare measurements with simulation results. However, adequate characterization of the grating is not a simple task. The experimental results are influenced by the accuracy of the fabrication as well as accuracy of measurements itself. For Smart Photonics MPW run 20 we prepared a series of DBR grating test structures which allow to:

- Determine the deviation of the spectral response of the gratings vs. geometry.

- Define a deviation of the effective index of the grating. This is necessary to have a link between the pitch and peak of the reflection band of the DBR grating.
- Choose an optimal method to obtain the absolute reflection spectra of the gratings. This can be used later on to characterize DBR gratings fabricated using scanner technology.
- Compare experimental and simulation results.

Moreover, the mask design includes test structures of various tuneable DBR-based lasers. Characterization of these tuneable lasers is a first step to include them into a library, e.g. the Smart Photonics PDK. Moreover, the results obtained from the characterization of these lasers will help in considerations for the other tuneable laser designs, namely hybrid low-linewidth laser and widely tuneable laser based on sampled gratings.

Milestone Summary (WP3.1.M1): Mask Design Tape-out I - Laser

We have designed a mask for examining performance of the DBR gratings (spectral response) and DBR based tuneable lasers. The results obtained after measurements of the test structures will:

- Allow quantification of DBR spectral response variation in gratings of the same pitch and length. This information is highly valuable for the PIC designers who are willing to use DBR gratings in tuneable lasers and for filtering purposes;
- By comparing measurements of the different test structures we can establish most reliable characterization technique, which in its turn can be used later on to characterize gratings fabricated using scanner lithography;
- Measurement results can be used to calibrate grating models, which can be included in the building block modules in circuit simulators.

Basic measurements of tuneable DBR lasers, e.g. LI curves, tuneability, and SMSR, will provide a quick indication of laser performance. In case the performance of the lasers is acceptable, i.e. a power >1 mW, and a SMSR>25 dB, these tuneable single mode lasers can be added to a library for the Smart Photonics process. In addition to this more advanced measurements on for example wavelength stability and RIN (noise) can be performed.

Report Summary (WP3.1.R1): Building Block Results I - Modulator

MZ modulator chips were fabricated in the SP20 B run and have been characterized with respect to their electrical and electro-optical behavior. The electrical results indicate a bandwidth of around 30 GHz. The measurements support and strengthen the insights gained from the simulations on the effect of geometrical parameter variation on modulator performance. The electro-optic large signal modulation experiments show only open eye diagrams until 20 Gb/s which is surprising given the measured bandwidth. Several possible causes have been suggested and further investigation is needed to determine the exact reasons.

Milestone Summary (WP3.3.M0.IT0): Report on Standard MPW BB Cell Results

One of the project's goals is to enrich the process design kit (PDK) of the regular multi-project wafer runs (MPW). For this reason test structures have been designed that contain basic building blocks (BBB) which are fabricated in each run, so that their performance can be

characterized. This will feed back to the improvement of the PDK. Among those test cells, there are also lower level test structures that assess more fundamental parameters of a MPW such as metal or planarization properties. Those are equally important for the PDK, especially for developers of more advanced components. In this report, we present measurement results of low-level test structures from MPW SP19 and SP21. It establishes design rules for small metal features and also presents their sheet resistance and RF behavior for either sputtered or electro-plated processes. In addition, the p-InP sheet resistance has been measured and planarization of polyimide on shallow and deep trenches was investigated. Further results on the contact resistance measurement structures are to be expected soon for other MPW runs and more insight into the planarization topology is expected.

Milestone Summary (WP3.3.M0.IT1): Report on Standard MPW BB Cell Results

A building block test cell has been designed and manufactured in a regular Smart Photonics MPW run. We focus on the electrical test structures that do not need optical fiber coupling, in specific the waveguide loss, SOA spectral gain and EOPM efficiency test structures. All three are intended to be probed with a multi-contact probe-card in the electrical domain and the relevant parameters shall be extracted from the purely electrical measurements. The procedures are detailed in report WP3.2.R0. Several new insights were gained from the current building block test cell that relate to challenges in the implementation of the measurement and the analysis of the measurement data. Those insights lead to modifications on the test structure design that was implemented in a revised building block test cell. Although electrical measurement of building block parameters remains a very attractive feat, its implementation is still challenging and further work within OpenPICs will explore the possibilities towards this goal.

Milestone Summary (WP3.4.DF.M1): Design Flow Improvements

In this report the following design improvements are described. The change is explained and the way to use it. The following improvements are addressed:

Including Modal Properties in PDKs, Available in OptoDesigner 5.2; Extend documentation of Black Box Handling (GDS + SPT), Available in OptoDesigner 5.2; Adding new classes for usability. Use case has been tested and initial documentation has been submitted. Autorouting, Available in OptoDesigner 5.2.

Report Summery (WP3.4.DRC.R2): DRC Implemented Improvements

For the OpenPICs project the following improvements in the area of DRC have been implemented:

1. Grouping of DRC rules.
2. Connectivity tests

The DRC grouping functionality is a way in OptoDesigner script to define, enable and disable groups of DRC rules. By doing so, the user can choose to only run a part of the DRC rules. This would significantly speed up correcting the user's design if running all DRCs at once takes long. DRC grouping can be done either using script commands or selecting specific groups in the graphical user interface.

A DRC group can be defined by the user, and subsequent DRC rules can be added to that group. Subsequently, by selecting one or more groups only those DRC groups will be run. It is also important to know that if specific groups are selected through script, this will take precedence over any GUI selection that the user has done.

Work Package 4 – Process Improvement

Milestone Summary (WP4.MS2.1): Investigation of Zn-diffusion for MPWs

In this report, the selective diffusion of Zinc is investigated. The target is to have a selective Zn diffusion process for the fabrication of active components in generic photonic integration, and eventually allow active-passive integration with very low loss passive waveguides.
Achievements:

- Diffusion in main materials of interest was investigated
- Diffusion was characterized with two different methods (CV and SIMS) for better understanding of electrically active Zinc
- Non-uniformity of Zinc diffusion over three inch wafer was measured
- Reproducibility issues of Zn diffusion were identified

Outlook

The OpenPICs project has recently passed the half-life mark and is approaching the end of the second year. Throughout all four work packages, it can be observed that the methodologies, created and drafted at the beginning of the project, had been implemented by now and initial results are available or being gathered. Valuable insight in operational aspects, process performance or promising results with respect to building blocks and new process technologies have been reported. The focus in the coming period will lie in addition to the defined demonstrator chips from Effect Photonics and Technobis, respectively.

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Introduction

This summary brief will give an overview of the activities carried out in the second half of 2018 within the Open Innovation Photonic IC project. The activities are divided between four work packages (WPs): Market Demand, Process Characterization, Building Block Improvement and Process Improvement. In WP1, we have continued to track performance metrics of the periodic photonic circuit fabrication runs of the open access pilot line. In addition, we are actively reaching out to new customers and engage them in technology development programs in case the open access offering is not matching their requirements. This led to the establishment of two new development projects (H2020 InPulse, OIP4NWE) and several programs in planning. In WP2, the fabrication processes have been tracked along multiple runs with respect to key metrics, so that statistical information is available on their stability. New developments are being worked on that improve process uniformity and wafer growth. In WP3, an automated die tester has been set-up that allows fast and efficient measurement of standard building blocks. Furthermore, we have established several novel high-speed components and improved the design workflow by adding standard interfaces for measurement data exchange. In WP4, we have developed etching processes for new material systems and optimized them to be used in coming device developments. In the following, summaries of the detailed work are given.

Work Package 1 – Market Demands

Milestone Summary (WP1.M4): Key performance Indicators for MPWs – Update

In 2018 TU/e received 67 requests for different services from multi-project wafer run (MPW) to packaging, 54 requests concerned participation in an MPW run (51 on InP, 3 on Si_3N_4). Customers were timely helped to get the necessary information to choose the most suitable foundry and submit their designs on time. No customer coming through JePPIX caused any delay in the start of MPW runs. In the past, the majority of customers for MPW runs came from universities, however, in 2018 half of the customers come from industry. This can be seen as a sign of industrial engagement in photonics and also as a result of successful dissemination made over the past few years. More than half of MPW run customers are from European organizations. In addition, in 2018 an increased interest from China and the United States of America has been observed.

Milestone Summary (WP1.M5): Training and Outreach – Update

The JePPIX Roadmap was officially release on March 11, 2018 at the OFC conference. This summary gives distribution statistics of the JePPIX roadmap since its release. In addition, it contains the results of a feedback survey that was performed after the annual JePPIX Training 2018. Participants were asked about their experience with the open access PIC training. The overall response indicates general satisfaction and high educational impact of the training. Dissemination activities are listed here for both JePPIX events and for presentations about technical aspects of OpenPICs.

Work Package 2 – Process Characterization

Milestone Summary (WP2.1-M1.3): Generic MPW Parameters Update Q4-2018

The goal is to track the MPW performance indicators over time and to improve the process stability. Various stability improvements have been introduced throughout the Smart Photonics fab. Some examples are listed below:

- Epitaxy: improved calibrations guarantee a more controlled photoluminescence response.
- Dry Etch: Improved recipe at the HTC fab shows less sloped profiles, 3x CD loss reduction
- WG loss: Since MPW SP21 the Deep WG loss performance is stable at 3.3 dB/cm
- Threshold Current: Passivation and polyimide improvements introduced in SP19&20 show stable thresholds, typically 25 mA/mm for All Active FP lasers.
- Extended Cavity Laser performance has been stabilized as well

Milestone Summary (WP2.2-M3.2): Dummy Structures / Tiling

The goal is to assess the effect of dummy structures / tiling on dry etch, the planarity and the general MPW performance. Test structures for the tiling have been designed:

- Small tiling array designed on SP24-B for planarity checks with 25-50-75% Pattern Density
- Similar tiling was applied to a Smart internal mask set with FP lasers for Cl2 Dry Etching

Typically, in the semiconductor world, for reasons of uniformity, tiling is within the 20-80% pattern density range. Global tiling density is typically applied on a 30 x 30 µm area. Depending on the technology and necessary performance, there are sub-criteria which are applied at smaller areas.

Milestone Summary (WP2.3-M1.1): Semi-Insulating Substrate

The goal is to verify the basic performance using semi-insulating substrates in the pilot fabrication runs.

- MPW-B runs using Semi-Insulating (SI) substrates were processed successfully, with typical performances similar to the MPW-A runs on S-doped substrates. Offering a SI process option is therefore considered to be low risk.
- No performance excursions were observed, except a slightly higher series resistance for the SI samples, which was expected.

Work Package 3 – Building Block Improvement

Milestone Summary (WP3.3.M0.IT2): Report on Standard MPW BB Cell Results – Die Tester

One of the goals within the OpenPICs project is to improve the Process Design Kit (PDK). Standard MPW building block (BB) cells are measured for this purpose in order to extract Figures of Merit (FoM) and gain insight into the building block performance. To obtain statistically significant results a large number of measurements is required. Thus, we aim to develop an automated die tester system that will routinely measure standard MPW BB cells and generate data that can be analysed to improve the PDK.

This milestone presents the capability of the die tester to perform electrical and optical measurements of photonic circuits in an automated way, taking the information from scripted files that follow an open standard. The infrastructure for high-volume BB characterization is established and gathering of statistical building block information can be tested.

Milestone Summary (WP3.3.M0.IT3): Report on Standard MPW BB Cell Results – MMI

One of the goals within the OpenPICs project is to improve contents of the Process Design Kit (PDK). An important piece of information contained in the PDK is the performance for each of the building blocks (BB). In order to enable the collection of statistical data for PDK population, an automated die tester has been developed over the past year, currently allowing for automated testing of passive photonic chips. One of the standard passive components which is widely used in Photonic Integrated Circuits (PIC) is a 2×2 3-dB MMI coupler. In this milestone we report measurement results on a test die containing a number of MMI couplers. The functionality of the automated die tester has been demonstrated with measurement of the MMI chip. The results show high stability and good repeatability of the optical alignment algorithm (within 0.02 dB). This allowed us to characterize the MMI couplers' performance and identify possibilities for utilizing a narrower and shorter MMI coupler than is currently in use. The MMI imbalance was determined to be between -0.6 and 0.6 dB.

Milestone Summary (WP3.1.M2): Mask Design Tape-Out II - Capacitively-Loaded CPW Modulator

The goal within the OpenPICs project is to develop modulator building blocks that can support 28, 56 and 112 GBaud operations. It has been initially identified in Milestone WP3.1.M0 that state-of-the-art bandwidths to support these symbol rates can only be achieved with capacitive loaded Mach-Zehnder modulator electrodes where a combination of velocity and impedance match can boost the high-speed performance. We have therefore adapted the design concepts readily discussed in the literature to the generic integration platform in OpenPICs to test the feasibility of such a modulator building block. We present the concept of the capacitively-loaded traveling-wave MZM (CL-TW-MZM), then go into details of the simulation results and show the final tape-out for the test structures in this milestone. The document details the second mast tape-out for the modulator building block development. Simulations have been

performed to synthesize optimum geometrical values and test structures have been designed for SP24-B to assess the performance of fabricated devices.

Report Summary (WP3.1.R1): Building Block Results I – RF Lines

Photonic building blocks often need electrical control and drive signals that are routed from the chip edge to where they are required. This electrical routing is realized in form of metal traces on the photonic chip. In case high-frequency or radio-frequency (RF) signals are needed, those routing lines need to support high frequencies. Until now, a standardized RF line building block does not exist in the generic integration platform, offered by Smart Photonics. Within OpenPICs, activities focus on developing such an optimized RF line building block that can be used by any designer. Suitable test structures of RF lines with varying dimensions have been designed as described in milestone WP3.1.M1 and have been manufactured in the SP 23 MPW run. In this report, we present the measurement results and an analysis of the optimum dimensions for such RF lines. The target was to gain insight into the main design variables of a CPW line and how those affect the performance of the line. We observed that both the signal and ground metal widths play an important role and synthesized recommended design values for an optimum CPW line.

Report Summary (WP3.1.R1): Building Block Results I – BCB RF Lines

This report presents the measurement results that were obtained for RF lines defined on a BCB passivation layer. The concept has been described in milestone WP3.1.R1 and was implemented on both n-doped and semi-insulating dummy InP wafers. The aim is to be able to define those structures in a post-processing step after a standard MPW run on top of the photonic structures in case high performance RF tracks are desired. In this report, we show measurement results of four different RF lines, realized on InP substrates with and without BCB. The results are very promising indicating > 67 GHz bandwidth for 1 mm long lines and show that the BCB process is attractive for creating low loss RF tracks on n-doped standard MPW photonics. This will also enable future extended flexibility for RF routing and interconnection of photonics with electronics.

Report Summary (WP3.4.EF.R0.IT0): Execution Flow

Testing of the photonic circuits plays an important role in the fabrication chain. The costs for testing can reach up to 30% of the total product costs. Testing is performed on different stages of the fabrication: from on-wafer testing during and after the fabrication to module-level testing of the packaged devices. The data generated during these measurements is heterogeneous, and is used for different purposes: pass-fail procedure, process control, device models development and calibration. This involves various parties, such as foundry, measurement labs, designers, and software companies which use different tools to generate and process the test data. This report describes the results of the activities towards standardization of the measurement / analysis data storage and exchange. The report consists

of two parts: the data file format description, and database design draft for storing the measurement data.

We have proposed a draft of the database schema for storing heterogeneous measurement data. The database can keep various metadata related to the design, fabrication, measurements, and the measurement data itself. This enables effective access to the data for complex analysis requiring connection of process and design parameters with the measured building block / circuit performance.

Report Summary (WP3.4.DRC.R2): Implementation of new DRC functionality

Many DRC operations can be executed in parallel to speed up the whole process. This is well suited for multicore processors. Multicore support has been implemented. It is not directly visible to the user but clearly visible in the calculation times for the DRC. A clear improvement going up to about 10 cores has been achieved. Above this number the overhead to manage the multiple cores starts to effect the speed, causing a flattening of the speed gain.

A new function was added in addition to check for short edges, abrupt jogs and sharp edges. More precisely, this DRC function gives a DRC error if both of the following conditions are met:

- an edge is shorter than the minimum length, and
- the two angles at both sides of the edge are larger than a maximum angle.

Work Package 4 – Process Improvement

Milestone Summary (WP4.MS1.2): Etching and passivation processes developed

The goal is to investigate fabrication methods that allow the etching of active waveguides based on Aluminium. This will be employed to fabricate the Al-based phase modulator. A strategy to fabricate waveguides without the need of dry etching has been identified. Waveguides will be fabricated with selective wet etching and the aluminium modulator will be based on ridge waveguides.

Milestone Summary (WP4.MS4.2): Etching process optimized

Waveguides etch is one of the most standard processes for the fabrication of Photonic Integrated Circuits. The quality of the etching profile (both in smoothness and etch depth accuracy) can be detrimental to both active and passive components. We performed experiments to fabricate passive waveguides with different etching processes. Measurements of the waveguide propagation loss allowed to quantify the results. The Fabry Perot method was employed for the transmission measurements of the waveguides.

Outlook

In the next period, which starts the final year of the OpenPICs project, each of the work packages will focus on its respective key goals. In WP1, we will further strengthen industrial collaboration and identify needed development areas in order to form open innovation projects. In WP2, gathering of statistical process parameters and continued improvement of the processes will be performed. In WP3, demonstrator circuits for both a datacom and a sensing application will be made whereas more advanced building blocks will be characterized and included into the MPW offering. Enhanced devices will be demonstrated with the newly developed modulator material within WP4 as a pre-cursor to technology enhancement of the pilot line.

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Introduction

This summary brief will give an overview of the activities carried out in the period 01/2019 – 12/2019 within the Open Innovation Photonics IC project. The activities are divided between four work packages (WPs): Market Demand, Process Characterization, Building Block Improvement and Process Improvement. This is the last summary brief for the OpenPICs project as it has ended with 12/2019 after a three year duration. Most of the work in the reporting period has focused on WP3 and WP4 where new results for building blocks, design flow improvement and process development is being reported. Together with the finalization of the process characterization of the generic MPW runs, it marks the end of this open innovation development project.

Work Package 1 – Market Demands

WP1 focuses on the market demand for photonic ICs and aims to create the link between market applications and the technology development. The work performed in this WP has led to several highlights throughout the project duration with all reporting having been finalized already within the previous reporting period. The activities in this reporting period continue the core lines of linking product demand to technology, developing roadmaps, performing trainings and gathering open access MPW run statistics.

Work Package 2 – Process Characterization

Milestone Summary (WP2.3-M1.4): Spot-size Converter Development

The procedure for including the spot-size converter process into the Smart Photonics platform has been captured. Several trial processes have been performed and the milestone describes the process, the PCM elements and resulting overlay data with SEM observations.

Work Package 3 – Building Block Improvement

Report Summary (WP3.1.R2): Building Block Results II – Modulator

This report describes the results obtained on the travelling-wave Mach-Zehnder modulators that use a more efficient EO material compared to the previously characterized modulator from report WP3.1.R1 Building Block Results I – Modulator. DC Switching characteristics with improved V_π and open eye diagrams up to 50 Gb/s are measured.

Report Summary (WP3.2.R1): PDK Upgrade with Advanced Building Blocks

This report summarizes the work performed to include newly developed building blocks into a process design kit (PDK) for easier use in future PIC designs. The PDK is implemented with the Nazca Design tool and adapted to the generic integration process. Both Mach-Zehnder type and electro-absorption type modulators have been implemented in this PDK.

Report Summary (WP3.2.R2): Compact Models

This report describes the status of compact model development for the description of the Building Blocks of the Smart Photonics platform. Compact model description of fundamental

building blocks, the shallow and deep waveguides have been created. A connection between fabrication parameters, variations and performance of devices have been established.

Milestone Summary (WP3.3.M1): Composite Building Block Test Cell Results

This milestone summarizes the results obtained from the composite building block test cell. The purpose is to capture the performance of composite building blocks in a standard MPW run. The reported results include that of the simple DBR laser and that of Mach-Zehnder and electro-absorption modulators.

Report Summary (WP3.4.DF.R2): Design Flow Improvement Points

This document describes the possible improvement points for the design flow. This is based on the design flow document WP3.4.DF.R1 and has been updated for the final version. Overall design flow work from Phoenix BV has focused on:

1. Modal properties as extension of the PDAflow
2. Black Box implementation
3. Auto-routing
a. Automatic insertion of crossings
4. Layout vs Schematic
5. Bi-Directional Interface

Milestone Summary (WP3.4.DF.M1): Implementation of Design Flow Improvement

Auto-routing has been implemented into OptoDesigner. The user simply sets up a grid, decides (for waveguides) what types of bends, straights and crossings to use, and defines pairs of ports in their design between which they want waveguide or metal connections to be made. OptoDesigner then attempts to create all connections. In addition, the OptoDesigner LVS (Layout versus Schematic) feature has been implemented and allows you to analyse the layout implementation of a photonic integrated circuit, and if a license to IC Validator is available, to do a rigorous check as to whether the implemented layout is functionally equivalent to the schematic as designed in Optsim Circuit.

Milestone Summary (WP3.4.DF.M2): Design Flow Bidirectional interface

To enable schematic design and simulation, PDK building blocks have a schematic representation with an associated model. To improve the design efficiency a bi-directional interface between the schematic and layout of the PIC design is a great improvement. This document describes the bidirectional interface to improve the design flow efficiency to enable information transfer of the schematic design to the layout design and back again.

Milestone Summary (WP3.4.DRC.M0.IT2): DRC Implementation in PDKs

The number of design variations for a photonic platform are countless and come from designers who do not necessarily know the details of the fabrication process. To ensure that the designs comply to the fabrication process, a list of design rules can be set. Once the design is made, a quick and efficient method to identify and notify for possible design mistakes is necessary. This

is called the Design Rules Checking (DRC). This report summarizes the DRC implementation for the development PDK of TU/e-PITC that is used to improve on photonic building blocks.

Report Summary (WP3.4.DRC.R2): DRC with strip tree

This document describes a major improvement in the DRC by using strip tree algorithms. Considerable speed improvement of the DRC checks was achieved using this algorithm.

Milestone Summary (WP3.5.M0): 400G Transmitter Design

This document describes the design of the transmitter demonstrator in WP3 of OpenPICs. Previously, a DBR-laser and a Mach-Zehnder modulator have been developed in WP3 and show good results for use in a transmitter application. The demonstrator design reported here uses those building blocks to construct a transmitter photonic integrated circuit which is compatible with the test assembly of Effect Photonics. This report presents the general architecture, the design and the used design procedure to obtain the transmitter circuit.

Work Package 4 – Process Improvement

Milestone Summary (WP4.M.1.1): Designed MQW characterized, shallow-etch modulators demonstrated AND

Milestone Summary (WP4.M.1.2): Etching and passivation processes developed: ready for MPW validation

The key technological innovations which target high speed modulators are aluminum-containing quaternary materials, a layer stack with a high number of quantum wells, and an additional wet etching step in the fabrication of the modulator waveguides. The first provides higher device speed and enables higher temperature of operation, the second provides a higher optical confinement which results in a higher modulation efficiency per unit length, and the third provides a robust fabrication method independent from the quality of dry etched sidewalls.

In this work we developed a technology targeting high speed, high efficiency phase modulators. This technology is based on a new layer stack with 25 quantum wells made of Al-containing materials, a new design of the modulator waveguide building block, and an extra wet etching step to fabricate the modulator waveguides. The fabrication run requires only one extra month of processing work to be fully completed. This new modulator technology is compatible with the standard generic integration, enabling the combination of this new building block with all other already existing ones from the platform.

Milestone Summary (WP4.M.3.2): RF line process validated in joint MPW

The goal here is to fabricate RF interconnects on BCB, on top of two fully processed SMART wafers. This way, it is possible to realize interconnects for broadband signal routing with lower RF losses. A novel type of BCB is used for this purpose that enables easy processing. Validation of the process is being carried out with the post-processing currently in the backend process

(coating still to be done). The devices under test include Mach-Zehnder modulators with a variety of low-loss RF waveguides enabled by the second metal plane.

Milestone Summary (WP4.M.4.3): DUV lithography introduced to Triplex platform

The objective of LioniX International is to validate TriPleX™ basic building blocks with a DUV stepper/scanner lithography process in order to get access to narrower linewidths for their waveguides and the possibility to fabricate sub-micron gratings. The process development of DUV lithography process for TriPleX was started with the goal to run the DUV process on the scanner equipment of the TU/e. Due to operational hurdles and technical incompatibilities it was decided within the project that the experimental work involving the TriPleX platform on 4" wafers could be performed elsewhere, at the Center of Micronanotechnologies (CMi) at EPFL. This tool, which is an ASML PAS 5500/350C DUV Stepper, is standard configured for 4" wafers. All process development can later on be transferred to TU/e. The reticles for test structures have been designed with the process on the DUV scanner developed. An engineering run where devices are fabricated in ongoing.

Milestone Summary (WP4.M.5.3): Stepper Lithography Introduction at Smart Photonics

To improve manufacturability and reduce manual handling, a resist track (RITE) and i-line stepper (ASML PAS5500) have been successfully installed and released at Smart Photonics' facilities at the High Tech Campus. Several developments have been performed and procedures were set-up to release the various resist track and stepper processes. Currently some 600 production wafer passes already went over the i-line stepper.

Project Impact and Conclusion

The OpenPICs project ran from the end of 2016 to the end of 2019, slightly more than a duration of three years. The project had an ambitious scope from the start covering a wide range of aspects related to photonic IC development and innovation. This included activities to capture and engage with the market demand of photonic ICs, its manufacturing and monitoring of these fabrication runs, the development of new and improved building blocks and also the exploration of novel integration processes for next generation photonic IC manufacturing. All these activities were undertaken within an open innovation framework, where consortium partners can exchange knowledge and information to accelerate crucial developments, making it a much more capable approach compared to traditional closed innovation.

The impact of the project has been substantial both in terms of international reach and technological outcome. Embedded within the Photon Delta eco-system, the project has helped laying the foundations of notable, internationally acknowledged initiatives. All project partners have been heavily contributing from the start to the integrated photonic system roadmap (IPSR-i) activity and in parallel to periodic JePPIX roadmaps that have been and will be released in 2018 and 2020. Tens of businesses are trained every year to work with photonic ICs in the

JePPIX trainings and outreach is conducted in many international photonics events. On the technology side, Smart Photonics has transitioned within the three years into regular MPW wafer runs that are characterized with verification reports. Integration of stepper and scanner lithography into the process has significantly improved on fabrication accuracy and control. Also Lionix has explored the advantages of scanner lithography within this project. New processes for the next generation platforms have been created, leading to the integration of new materials, new substrates, new building blocks for faster and more efficient photonic ICs. A framework for automated photonic IC testing has been established with the partners, the first for generic foundry photonics, and successfully transformed into standards as listed on openEPDA.org. The testing capability are further taken up in initiatives such as EU H2020 Pixapp and InPulse and have been already used within the consortium. Improvements on design tools have been made with special emphasis on interoperability between such tools. Standards set there are used as a base line in new activities in the InPulse pilot line and have been instrumental for the advancement of photonic IC design flow in the community.

Although the majority of the project goals have been achieved, not all targets were met. One of such are the demonstrator circuits. For both user companies, the demonstrators have been fully designed but its fabrication is now still on-going which is due to the fact of previously reported delays in the integration of new cleanroom tooling. Furthermore, the initial project goals included metrics on extremely low linewidth lasers, ultra high-speed modulators and ultra low-loss optical waveguides. Some of those metrics could not be met as the consortium decided to focus the effort on core activities as reported.

Overall, the project has resulted in many important outcomes which elevate the state, maturity and performance for photonic ICs. It enhanced the collaboration between the partners and within the Dutch and European photonics eco-system, opening a route to broader adoption of open innovation in technology development.

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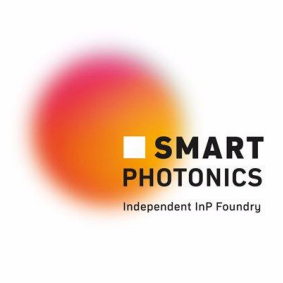
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